NASA CR-144983

DEVELOPMENT OF A HIGH CAPACITY BUBBLE DOMAIN MEMORY ELEMENT AND RELATED EPITAXIAL GARNET MATERIALS FOR APPLICATION IN SPACECRAFT DATA RECORDERS

ITEM 1

Development of a High Capacity Memory Element

By

P. J. Besser, et al

March, 1977

Prepared under Contract NAS 1-12981
by
Rockwell International Corporation
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COVER

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Development of a High Capacity Memory Element

16. Abstract

The objective of Item 1 was to demonstrate the availability of a bubble domain technology suitable for fabricating high capacity memory elements for use in spacecraft data recorder systems. The primary program effort was directed toward the development of a 102,400 bit bubble domain memory element and the demonstration that the developed device is capable of meeting the performance and cost goals of NASA data recorder systems.

Accomplishment of the program objective required developmental efforts in the areas of large capacity device design, bubble domain mask fabrication, large area high resolution device processing, chip packaging, yield modelling/analysis and large capacity device characterization techniques.

Several versions of the 100K bit chip, which is configured as a single serial loop, were designed, fabricated and evaluated. Design and process modifications were introduced into each succeeding version to increase device performance and yield. At an intrinsic field rate of 150 kHz the final design operates from -10°C to +60°C with typical bias margins of 12 and 8 percent, respectively, for continuous operation. Asynchronous operation with first bit detection on start-up produces essentially the same margins over the temperature range. Cost projections made from fabrication yield runs on the 100K bit devices indicate that the memory element cost will be less than 10 millicents/bit in volume production.

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FOREWORD

The work on Contract NAS1-12981 was divided into two separate but concurrent efforts, Item 1 and Item 2. This report covers the work performed on Item 1 during the interval 18 February 1974 to 31 October 1976. The results of Item 2 have been reported previously in NASA-CR-144960 dated June 1976.

The contents of this report represent the contributions of many individuals. Dr. P. J. Besser, Staff Scientist, Applied Magnetics Department was Principal Investigator on the program. Program responsibility was assigned to the Applied Magnetics Branch of the Physical Sciences Department, Mr. J. L. Archer, Manager. The bulk of the program effort was distributed between four groups of the Applied Magnetics Branch: Magnetic Circuits, Mr. R. F. Bailey, Group Leader; Microfabrication Techniques, Mr. J. P. Reekstin, Group Leader; Magnetic Devices, Dr. L. R. Tocci, Group Leader; Magnetic Systems, Mr. J. E. Ypma, Group Leader, and one group of the Materials Research Branch: Garnet Film Processing, Mr. R. G. Warren, Group Leader. Other individuals who made significant technical contributions to this program and their areas of effort are: Material Processing — Mr. T. N. Hamilton, Mr. R. Mendoza, Mr. D. Medellin, Mr. E. F. Grubb and Mr. A. J. Riccio. Device Processing — Ms. B. F. Decker, Mr. P. E. Elkins, Mr. E. F. Grubb, Ms. N. L. Lind, Mr. T. R. Oeffinger and Ms. C. D. Sallee. Device Design and Characterization — Mr. A. G. Campbell, Dr. T. T. Chen and Mr. J. L. Williams.

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ITEM 1

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Rockwell International

1. INTRODUCTION

This contractual effort was one segment of an overall NASA program effort directed toward the development of an all solid state replacement for the tape recorders presently used for data storage in spacecraft. The program has encompassed the entire range of bubble domain memory technology: materials research, system feasibility demonstration, material/device interface studies, chip development and prototype data recorder development. The primary contractual segments of this program are shown below:

Title	Contract	Final Report No.
Investigation of Chemical Vapor Deposition of Garnet Films for Bubble Domain Memories	NAS1-11446	NASA-CR-132325
Investigation of the Growth of Garnet Films by Liquid Phase Epitaxy	NAS1-11794	NASA-CR-2413
Investigation of System Integration Methods for Bubble Domain Flight Recorders	NAS1-12435	NASA-CR-132643
Conceptual Design of a 10^8 Bit Magnetic Bubble Domain Mass Storage Unit and Fabrication, Test and Delivery of a Feasibility Model	NAS8-26671	NASA-CR-123577

Title	Contract	Final Report No.
Development of a High Capacity Bubble Domain Memory Element and Related Epitaxial Garnet Materials for Spacecraft Data Recorders	NAS1-12981	
Item 1 — Development of a High Capacity Memory Element		NASA-CR-144983
Item 2 — The Optimization of Material Device Parameters for Application in Bubble Domain Memory Elements for Spacecraft Data Recorders		NASA-CR-144960
Solid State Spacecraft Data Recorder (SSDR)	NAS1-14174	Phase I Due 7/15/77 Phase II Due 4/15/78

The objective of this Item of Contract NAS1-12981 was to demonstrate the availability of a bubble domain technology suitable for fabricating high capacity memory elements for use in spacecraft data recorder systems. To provide criteria by which the accomplishment of this objective could be determined, certain specific device performance and cost goals were established as targets. The task structure of the contract was designed to provide a logical progression of effort culminating in a final chip design, the demonstration of its performance and an evaluation of the overall device yield.

It was convenient to organize the Item 2 report on a Work Statement Task basis but the nature of the Item 1 work does not lend itself so suitably to such an organization. Rather, this report is organized into various areas of effort which were necessary to effect the eventual goal of the program.

The approach to achievement of the memory element goals was the design, fabrication and detailed characterization of a series of chips, ranging in capacity from 1K bit to 100K bits. Design reviews were conducted after evaluation of each chip and modifications introduced to improve the performance of the succeeding design. The final version of the 100K bit chip is a two level, 16 μm period, serial loop design using T-bar storage, chevron based input/output elements, conductor loop generation/annihilation and passive replication of the data to a guardrail detector.

The initial contract called for two yield runs to provide data for yield/cost projections on large capacity memory elements. All process steps were reviewed after the first run and the sources of yield loss analyzed. Process modifications to improve the yield were incorporated in the second yield run and a resulting yield improvement was achieved. This improvement occurred even though more stringent device acceptance criteria were applied in the second yield run. Cost projections based on these runs and subsequent device fabrication indicates that the NASA system cost goals can be met by the available bubble domain technology.

In order to assess the criticality of chip matching for multichip package designs such as proposed for the SSDR system an additional fabrication run was made to provide devices for 8-chip memory cells in which all memory elements operate in common

bias and drive fields and share common control electronics. This device fabrication task is called the third yield run in the remainder of this report. These studies confirmed that chip matching for multichip packages could be performed with reasonable yields. The number and schedule of the matched chip set deliveries was altered as a consequence of a fire which occurred in the bubble domain device processing area of the Applied Magnetics Department on 29 May 1976. The fire-induced delay in this program and the continued progress on the 16-chip cell development phase of the SSDR program made the delivery of 8-chip cells on this contract less meaningful. Consequently, the matched sets of chips were delivered to the SSDR program for incorporation into the early deliverable cells on that contract.

The sophistication of the device evaluation capability, both wafer level and die level, increased dramatically throughout the duration of the program. Along with this evolution in characterization capability came a more exacting set of acceptance criteria for "good" devices. However, the improvements in material quality, device design, mask technology and device processing were more than sufficient to offset the more demanding chip acceptance requirements. As a consequence the overall yield of devices, even in the face of monotonically increasing performance demands, has continually increased throughout the program.

The objective of this Item has been fulfilled and it has been demonstrated that the bubble domain technology for fabricating high capacity memory elements for spacecraft data recorders is available. High performance 100K bit chips have been fabricated at yield levels which make the NASA system cost goals attainable. It has been a significant accomplishment to demonstrate this capability. Extension of the state-of-the-art was required in the areas of mask technology, large area-high resolution device processing, in-process testing, asynchronous-operation chip design, chip matching, and material fabrication. However, these advances were made and have resulted in the demonstration of a high capacity memory element capable of meeting the performance and cost goals for NASA solid-state data recorder systems.

2. HIGH CAPACITY DEVICE DESIGN

2.1 Introduction

2.1.1 Objective. - At the start of this program (February, 1974) the largest bubble domain memory elements available were approximately 10K bits having bit densities of only 160K bits/cm^2. Employing a chip of this capacity in a 10^8 bit system would seriously reduce the Mean Time Between Failure(MTBF) and result in an unacceptable system size and weight. The objective of this task was to design, fabricate and evaluate a chip with at least 100K bits capacity and a bit density so that only about 1000 such chips would be required in a 10^8 bit system.

A key initial decision in the chip development program was the selection of the chip organization to meet the memory element performance goals listed in Table 1. The serial FIFO (first-in, first-out) requirement can most easily be implemented by the simple single loop chip organization

Other advantages of the simple loop are its maximum ultilization of the garnet area, component simplicity, simplified device processing and ease of testing. These considerations made the simple loop chip an attractive choice for the 100K bit memory element organization. The major disadvantage is that the processing yield of a 100K bit serial loop chip is not expected to exceed~25 percent. (see Section 6.1)

Consequently, at the start of the program a detailed evaluation of the various chip organization candidates was made with regard to the performance and cost goals of NASA. It was concluded that any realistic alternative to the serial chip should incorporate some redundancy in the design. Redundant designs have the primary advantage of increased device processing yield. However, redundant approaches lead to reduced bit density per chip and increased complexity in component design, mask fabrication, processing and device testing. If on-chip correction is to be implemented the modification yield must be extremely high for the redundant chip cost to approach the cost of the simple loop. (Ref. 25) Off-chip correction requires greater system electronics complexity, hence increased parts count.

Consideration of the various tradeoffs involved at the time of the program start lead to the conclusion that the simple loop was the most promising chip organization for this program.

The maximum frequency and the temperature range shown in Table 1 are within the capability of the Ga-substituted class of bubble garnets that were used on this program. The final composition was a YSmGaIG which is discussed in detail in the final report on Item 2 (Ref 1). Nonvolatility is an intrinsic property of bubble memory devices and thus was one of the easier requirements to meet. One of the more difficult ones was first bit read upon startup which not only taxes the device design and the material but also the system electronics. In the final chip design all the goals listed in Table 1 were achieved except for the Operating Drive Field.

2.1.2 Approach to a 100K Bit Chip Design. - The bit density of the device is primarily limited by the resolution of the photolithographic mask and device processing technology and by the device component design. At the beginning of the program the minimum resolution that could be routinely attained in our labs was ~1.2 μm. How-

ever, by the end of the program this was reduced to 0.9 μm. The T-bar pattern was chosen as the basic propagation component for the chip since it was deemed to be the best available one at the time. The minimum feature for this pattern is the gap between the T and the bar. For a 1.2 micron gap the period should be about 20 μm. However, since the chip area at program start could only be 6.35m x 6.35 mm, as dictated by the mask fabrication process, the chip capacity for a 20 μm period would be limited to about 80K bits assuming that 15 to 20 percent of the area is required for input/output circuitry. In order to achieve the 100K bit capacity the period was reduced to 16 μm (3.9×10^5 bits/cm^2) which meant that the 1.2 μm gap was not quite optimum. In later chip designs, however, smaller gaps were achieved which resulted in improved performance over the earlier designs. Rockwell's approach to developing the 100K bit chip with a 16 micron period was to design and evaluate a number of chips culminating in the optimum design based on the state-of-the-art for device design and the mask and process technology. Each chip and its characteristics will be discussed in detail in Para 2.2. For an overall perspective the development sequence is summarized in Table 2. The details of the revisions mentioned will be explained in the following sections of this chapter.

TABLE 1. DEVICE PERFORMANCE GOALS

Organization	Serial, FIFO
Storage Capacity	≥100 K bits
Intrinsic Data Rate	150 kHz
Asynchronous Operation	0 to 150 kHz, start/stop
Temperature Range	-10°C to 60°C
Survival (with data loss)	-65°C to 125°C
Operating Margin	8 to 10% at 60°C
Operating Drive Field	30 Oe
Detector Output	0.5 mV at 2 mA; 15dB minimum signal to noise
Read Mode	Nondestructive; 1st bit read
Storage Retention	Nonvolatile
Bias Field	≤200 Oe

TABLE 2. DEVELOPMENT SEQUENCE

Device	Purpose	Revisions	Performance		Comments
			H_D min (Oe)	ΔH_B at H_D (Oe)	
1K Bit, 2-Level, M-1049	Evaluate design, mask fabrication and processing	First Chip	50	12.5/80	High drive field
1K Bit, 1-Level	Evaluate single level	Only Chip	—	—	Poor performance due to 1-level annihilator
100K Bit, M-1050	First Yield Run	Expansion of M-1049	70	10/80	High drive due to gap and line width dimensions
Partially populated 100K Bit (10K Bit) M-1057	Evaluate new design and new mask fabrication technique	Design Revision #1 1. Smaller gap and linewidth 2. New corners 3. Longer detector stretch	—	—	Device never completed due to mask procurement delays but design realized in M-1061
100K Bit, M-1061	Second Yield Run	Expansion of M-1057	45	12/50	Vastly improved drive requirement for ~10% margin
10K Bit, M-1064	Evaluate passive replicator and guardrail detector	Addition of passive replicator			See Item 2 final report Components similar to M-1061

TABLE 2. (Cont)

Device	Purpose	Revisions	Performance (30°C)		Comments
			H_D min (Oe)	H_B at H_D (Oe)	
100K Bit, M-1065	To eliminate annihilator delay	Design Revision #2 1. Smaller gap and linewidth 2. Add passive replicator 3. Horizontal guardrail detector 4. Slight modification to corners 5. Generator conductor loop shortened 6. Annihilator conductor loop alignment shifted	40	13/50	Passive replicator limiting component; more reliable generation; wider phase margin for annihilator
100K Bit, M-1066	Backup chip with in-line detector	Similar to Revision#2 with in-line det.	—	——	Chip never fabricated
100K Bit, M-1067	Evaluation, especially for 1st bit detection in asynchronous mode	Revision #2 design with vertical guardrail detector	40	12/50	Good first bit detection
100K Bit, M-1067B	Final Chip Design	Revision #3 detector feedthrough modified	40	12/50	Feedthrough modified to improve high temperature operation.

2.1.3 Material Considerations. - A number of Ga-substituted garnet compositions have been evaluated on this program and reported in the Item 2 report (Ref 1). Although some were superior in certain properties, such as mobility, than YSmGaIG, this composition was chosen for the chip development task because it is a basically simpler composition (fewer constituents) to grow than the other compositions evaluated. Since this composition has been used on many in-house programs a large amount of experience has been accumulated in growing uniform, low defect density, high quality films. This material is adequate to meet the chip performance goals listed in Table 1 although a greater safety margin would have been desirable at the high temperature end of the operating range. Successful operation with the YSmGaIG has been achieved at temperatures up to about 70°C, but this appears to be the limit for this material composition because of the reduction in margin due to decrease in bubble diameter and wall energy and a reduction in sense output as a result of the decreasing $4\pi M$. At low temperatures reduced mobility may cause some degradation. However with this material there seems to be no problem in reliable device operation at -10°C.

For a wider temperature range of operation it may be desirable to utilize one of the CaGe-substituted garnet materials. These compositions were excluded from the Item 2 study to avoid duplication of other contractual efforts (Ref 1).

2.2 Chip Development

This section describes the various chips that were designed and evaluated in the effort to develop a 100K bit chip meeting the requirements in Para 2.1.1. Space limitation prevents all the data from being included but where it was particularly significant to the task progress and direction these data will be reviewed. Characterization data on the final 100K bit chip designs are given in Section 7. Considerations leading to the choice of various components and chip designs are presented in Para 2.3. Table 3 summarizes the various designs and design parameters for each of the chips and Figures 1, 2, and 3 show the component designs for three of the chips representative of the chip development.

2.2.1 1K Bit Chip. - At the start of this program most standard bubble domain memory elements employed a 24 μm period. In order to make a 100K bit chip using the photolithographic equipment available at that time required that the period be 16 μm (Para 2.1.2). An experimental 1024 bit device with a 16 μm period has been designed, fabricated, tested and delivered (Oct 1973) under contract NAS1-11446 (Ref 2) to show the feasibility of going to the increased density. The purpose of the 1K bit chip investigated on this contract was to evaluate the various aspects such as component design, mask fabrication techniques, and device processing for this period. Based on component designs available at the program start the outer corner used was the bent-H type and the inner corner was an X-bar type. The outer corner defined as a 180 degree corner in which the bubble propagates around the corner in the same sense as the rotating field while for the inner corner the bubble propagates in the opposite sense. (All the components for M-1049 are basically the same as the 100K bit chip, M-1050, Figure 1.)

TABLE 3. DEVICE DESIGN SUMMARY

Tab 3

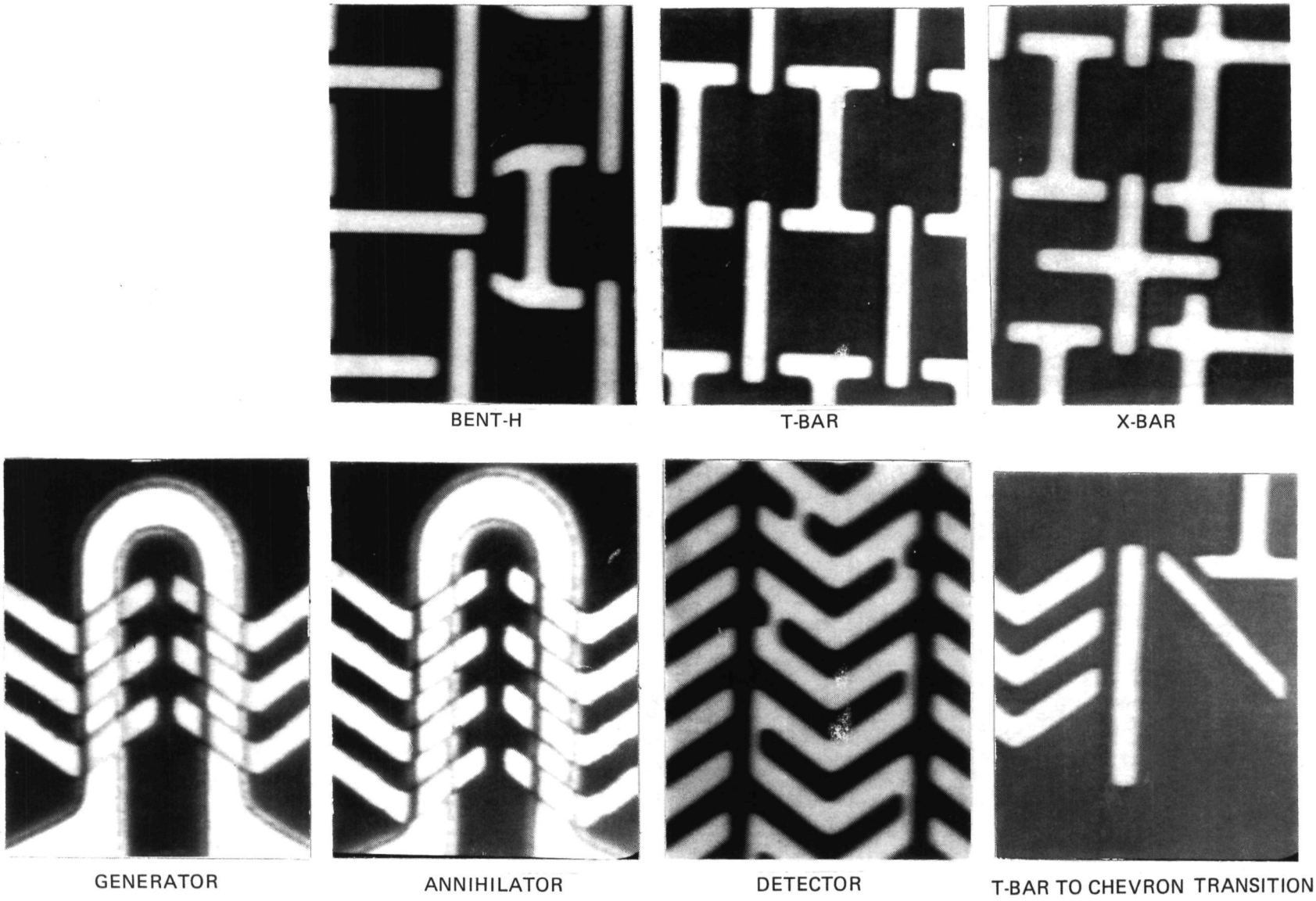

Figure 1. M-1050, 100K Bit Component Design

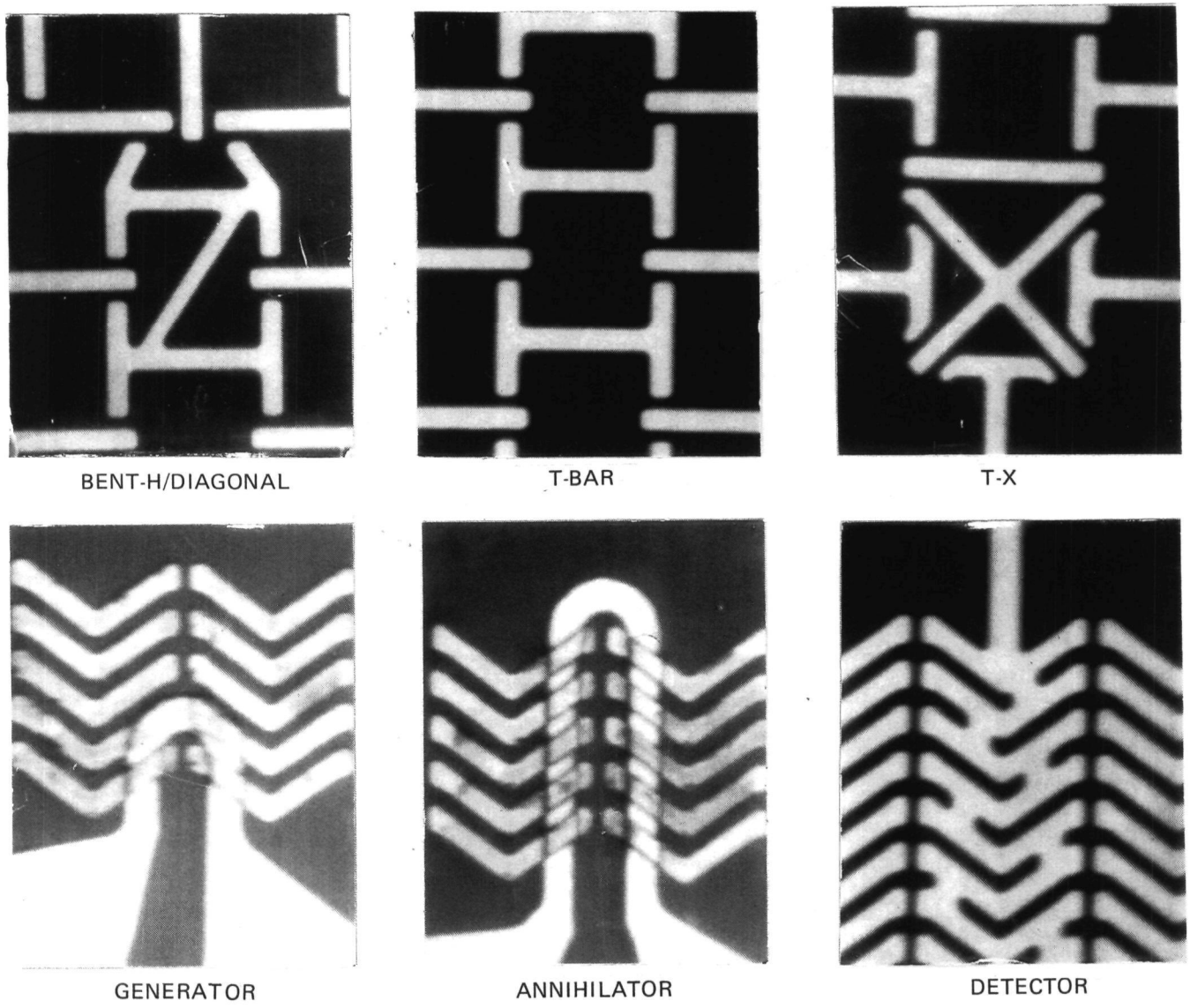

Figure 2. M-1061, 100K Bit Component Design

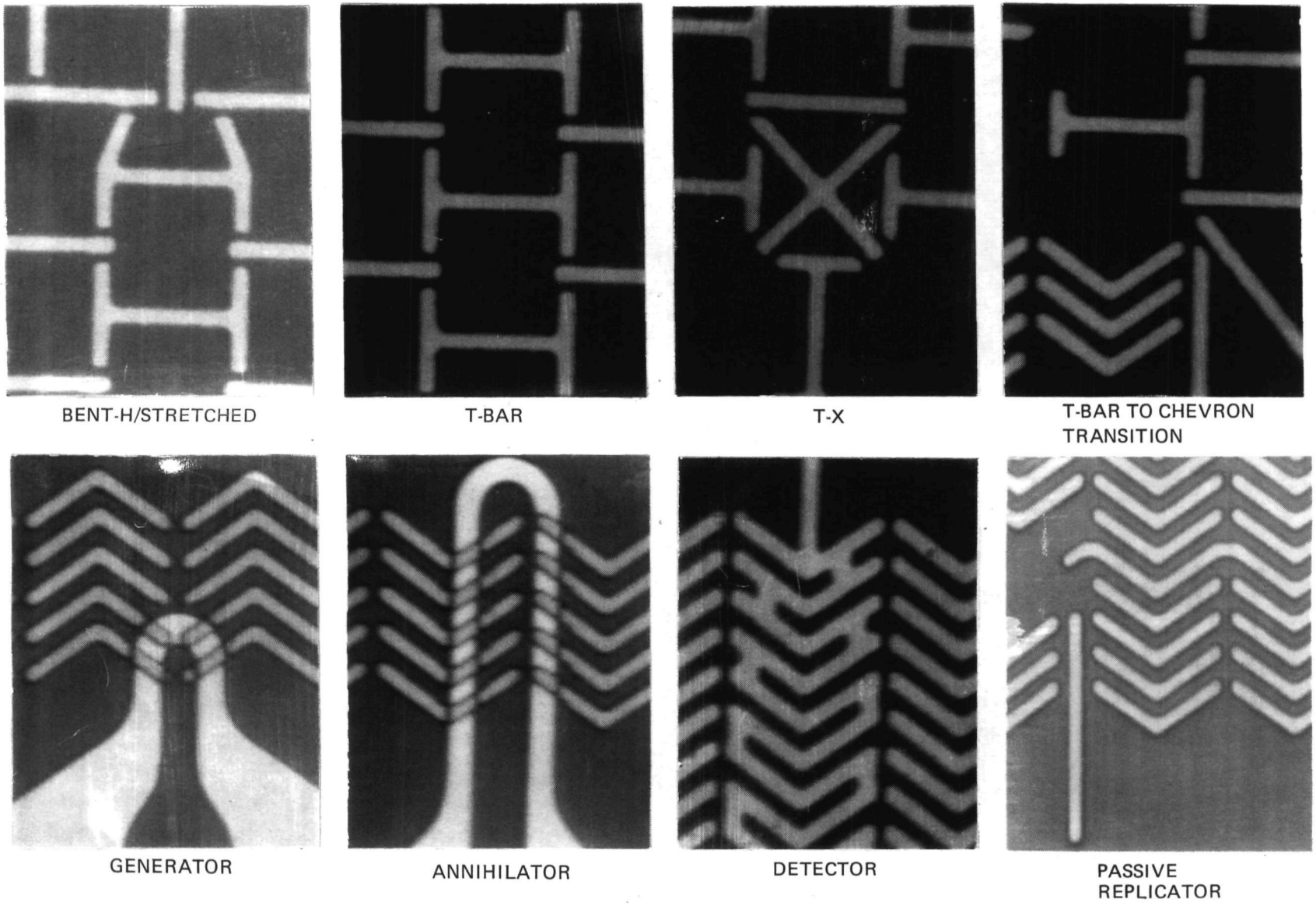

Figure 3. M-1067 100K Bit Component Design

For the permalloy propagation layer (p-layer) the linewidth and gap dimensions were chosen on the basis of the processing requirements. From the standpoint of optimum device design it was desirable to have gaps of about 1 μm and linewidths of about 2 μm. However, significantly different values were used to accommodate the existing mask fabrication and device processing constraints. The drive fields required for reliable operation of this chip were much higher than expected ($H_D \simeq 80$ oe). At first the high drive field was thought to be due to the corners and/or the transitions between the chevron and T-bar tracks. Normally, higher drive fields are required for these elements and it was assumed that the basic designs were at fault. In reality it was probably due to the less than optimum gap and linewidth dimensions, but this fact was only really apparent after the first 100Kb chip (M-1050) was made.

The generator and annihilator for this chip are of the commonly used conductor loop design fabricated with conductor first processing techniques. The current pulses required for generation and annihilation are similar for all the chips. Typical values are given in Section 7. Generation and annihilation phase margins were both quite adequate for this chip (each >180 deg).

The single level chevron stretcher type magnetoresistive detector was employed in all the chip designs but differed in the feedthrough design and the particular chevron shape and shorting elements. All the detectors were of the end-shorted zig-zag type. The detector in this chip had only a 30 element stretch resulting in a detector sensitivity of ~100 μv/ma at room temperature. This value was somewhat smaller than desired. In all of the chip designs the active detector forms one arm of a bridge circuit which is completed by the dummy detector and fixed resistors. Thus the current supplied to bridge is twice that which flows through the active detector. The detector sensitivity values which are given throughout the report are based on the current through the detector, not on the bridge current.

The layout of this chip was such that the propagation direction in the T-bar storage region was parallel (or antiparallel) to the propagation direction in the chevron track. This leads to poor start/stop characteristics for this chip (see Para 2.2.4 and 2.3.1.3).

A single level version of this 1K bit chip was made to evaluate this technology as single mask processing is more attractive than two-mask processing. A disk type active generator was employed along with a single level version of a conductor loop annihilator. The chip did not operate reliably because of a faulty annihilator design. It was concluded at this point that it would be wisest to concentrate solely on the two level approach rather than modifying the one level design since the one level approach was not a necessity to achieving the desired cost goals for this bit density and two level designs were more advanced.

2.2.2 100K Bit Chip, First Version, M-1050. - This chip (Figure 1) is essentially an expansion of the 1K bit chip (M-1049); however, the pattern was generated by flashing complete rectangular bars and elements rather than by painting. The term painting here refers to a photo plotting technique where an aperture is translated during exposure to generate a bar pattern. This chip also required very high drive fields (~80 Oe) for reliable operation just as found for the M-1049 chip. Device measurements on in-house test circuits indicated that it was not primarily the type of component designs that were causing the poor performance, rather it was found that the large linewidth and gap dimensions were primarily the cause. A new, more precise way had to be found to

generate the patterns for mask fabrication and device processing had to be improved so that smaller gaps and narrower lines could be employed in the design.

2.2.3 Partially Populated 100K Bit Chip, M-1057. - At this point in the program a new capability for mask fabrication became available, the Mann 3000 pattern generator. The Gerber photoplotter used for the previous chips was a machine primarily designed for circuit board layouts. It was replaced by this newer, sophisticated, more accurate pattern generator (Section 5.3) for designs subsequent to M-1050. With the capabilities of the Mann machine and other processing improvements the linewidth and gap dimensions were reduced. A partially populated 100K bit chip was designed to evaluate the new fabrication methods. Although this chip was never completed because of various delays, considerable experience of value to the later work was obtained from this attempt.

2.2.4 100K Bit, M-1061. - This chip (Figure 2) is an expansion of the partially populated chip mentioned in the previous paragraph. Modifications included in this chip were reductions in linewidth and gap in keeping with improvements in mask and device fabrication, rotation of the T-bar storage region by 90 deg to improve start/stop operation and use of a bent-H corner with a diagonal bar and a T-X type corner. As a result of the design changes, especially to the gap dimension, the minimum drive field was reduced to 45 Oe with a 10 percent margin available at 50 Oe as opposed to 80 Oe for the earlier design. A factor of three increase in detector output was achieved by increasing the stretch to 100 chevrons. Along with the other dimensional reductions the stacking distance of the chevrons was reduced from 3 microns to 1.5 microns. This closer spacing probably also helped in reducing the drive field, especially in the detector area.

2.2.5 10K Bit Test Chip, M-1064. - For an in-line detector layout there is always a delay between detection and annihilation approximately equal to the stretch of the detector since the stretch can only be decreased by one chevron per period. Zero delay between all the input/output functions is especially desirable because of the simplicity it permits in the system hardware and logic. One method to achieve coincidence of the generation, annihilation and detection functions is to use a replicator component in the storage track which feeds a duplicated data stream into a guardrail chevron detector. In this manner the distance in bit steps between each function can be adjusted to obtain zero delay.

Although active replicators such as the pickaxe (Ref. 3) probably have better margins, a passive replicator design was deemed best for this program since it did not require any additional leads, bonds or associated electronics. Several different designs were evaluated in the Item 2 portion of this program (ref 1). One design was employed in a 10K bit chip to prove the concept. This chip is discussed in detail in the Item 2 report along with the passive replicator. Some additional data on the passive replicator is shown in Para 2.3.3. As a result of the reasonable performance characteristics, it was decided that this approach would be used in a 100K bit device.

2.2.6 100K Bit Chips, M-1065, M-1066, and M-1067. - The three devices discussed here represent a family of chips employing an additional reduction in the linewidth and gap dimensions, an improvement in the Mann flash composition of the T-X corner, modifications to the chevron-to-T-bar transitions and a reversion back to the bent-H corner without a diagonal bar (Figure 3). The reduction in the linewidth and gap dimensions were in keeping with the effort to optimize the device geometry for the

16 μm period and were made possible by further improvements of mask and device processing. In several cases other than just the T-X corner the flash composition of a component had to be modified or rearranged somewhat to improve the resulting pattern; however, the basic design of the components was in general not altered.

Schematics of the three chips are shown in Figure 4. The second device, M-1066, which did not employ the passive replicator was considered as a backup chip and was never completed in light of the performance of the other two chips. The first device M-1065, represents the logical placement of the detector in the guardrail (i.e., horizontally in reference to Figure 4.) The storage area was laid out such that the start/stop direction of the in-plane field for asynchronous operation was parallel to the bars in the T-bar storage region which would place a stopped bubble in the chevron gap of the detection region. Based on other measurements (Para 2.3.2.2) it was suspected that stripout of the domain could not be achieved for this start-stop direction in the detector to reliably perform first bit detection upon startup, even with the application of a small inplane holding field or a precharge delay of the driving field. Since first bit detection had been successfully achieved with the in-line design (vertical orientation such as for M-1066 in Figure 4), device 1067 was designed with the vertical detector orientation as well as the passive replicator for input/output coincidence. Complete performance data of the M-1067 design is given in Section 7.

2.2.7 100K Bit Chip M-1067B. - The feedthrough for the detector of device M-1067 (as well as 1065) is curved as it enters the guardrail (Figure 5). Quasistatic data showed that at low bias the domain that had just passed through the detector could strip back into the sensor through the top feedthrough especially in start-stop operation. In hind sight it is obvious that propagation along the top feedthrough path is favored by clockwise field rotation. Since the failure was more likely to occur a higher temperatures where the wall energy is lower and the wall mobility is higher it was felt that the feedthrough should be modified to minimize the occurrence of this effect. The modification was such that between the guardrail and the detector the feedthrough was straight and at least two periods long. The straight design does not allow a driving force large enough to cause the domain to stretch back into the detector unless the bias is so low as to cause stripout failure in other parts of the chip.

Device 1067B is the final version of the 100K bit large capacity chip developed on this program. It meets every requirement listed in Table 1 except the drive field. However, it should be noted that part of the reason for the higher drive field is the large physical area of the chip and the fact that it is serial. For this large area the probability is high that minor defects or variations either in the garnet or due to processing will occur within the chip area. Higher drive will be required to propagate the bubbles past them. Of course the individual component designs are also important in determining the drive field requirements and the overall chip performance. For this design it is the passive replicator that limits the low drive end of the margin. (see Para 7.2.4) In a very small capacity device of the same T-bar design (without a replicator) with no apparent minor defects the minimum drive field measured was only 25 Oe, quite a bit lower than the initial goal for the 100K bit chip.

2.3 Component Designs

2.3.1 Propagation Elements — Storage Region. - The T-bar (or H-bar) pattern was chosen for the storage region since it exhibited better performance over the other commonly used pattern, the Y-bar. The poorer propagation characteristic of the Y-bar could result from the weak pole position at the tail of the Y. Since the T-X and X-bar

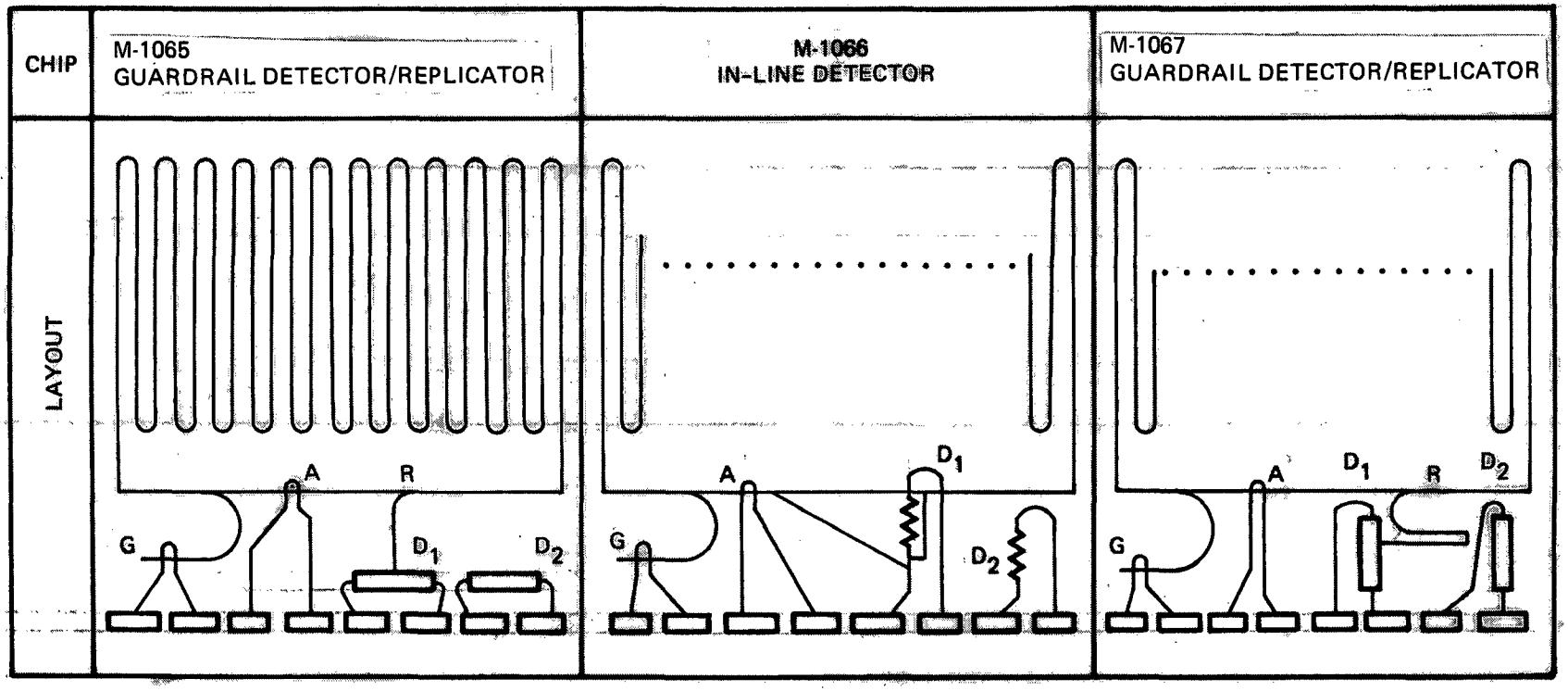

Figure 4. Schematic Comparison of Versions M-1065, M-1066 and M-1067

Device	Design Parameter			Corners		Detector			Generator		Annihilator		Pattern Generator
	λ	w	gap	Inside	Outside	Type	Stret.	Stack Space	Length	Delay	Align	Delay Steps	
1. 1Kb, 2-level M-1049	16.4	3	1.2	X-bar	BH[1]	I. L.	30	3.0	L	—	C	—	Gerber (painted)
2. 1Kb, 1-level	16.4	3	1.2	X-bar	BH[1]	I. L.	30	3.0	L	—	C	—	Gerber (painted)
3. 100Kb, M-1050	16.4	3	1.2	X-bar	BH[1]	I. L.	30	3.0	L	~30	C	~30	Gerber (flashed)
4. Part. Pop 10^5 (10Kb) M-1057	16	2.2	1.0	T-X[1]	BH/D[1]	I. L.	100	1.5	L	0	C	~112	Mann 3000
5. 100Kb, M-1061	16	2.2	1.0	T-X[1]	BH/D[1]	I. L.	100	1.5	S	0	C	~112	Mann 3000
6. 10Kb, M-1064	16	2.2	1.0	T-X[2]	BH/D[2]	G. R.	300	1.5	L	0	C	~50	Mann 3000
7. 100Kb, M-1065	16	2.0	0.8	T-X[3]	BH[2]	G. R. (H)	100	1.5	S	0	D. S.	0	Mann 3000
8. 100Kb, M-1066	16	2.0	0.9	T-X[3]	BH[2]	I. L.	100	1.5	S	0	D. S.	~107	Mann 3000
9. 100Kb, M-1067	16	2.0	0.9	T-X[3]	BH[2]	G. R. (V)[1]	100	1.5	S	0	D. S.	0	Mann 3000
10. 100Kb, M-1067B	16	2.0	0.9	T-X[3]	BH[2]	G. R. (V)[2]	100	1.5	S	0	D. S.	0	Mann 3000

Superscript denotes design version of component
BH/D — Bent H corner with diagonal bar
I. L. — In Line
G. R. ( )— Guardrail detector in horizontal or vertical orientation (see Figure 4)
L — Long loop covering all chevrons
S — Shorten loop covering one chevron
C — Centered on chevron gap
D. S. — Shifted Downstream

patterns had only recently appeared at that time they were bypassed in favor of the more standard T-bar. In any case the newer T-X and X-bar patterns would have been more difficult to compose using the present pattern generation techniques because of the angular orientation of the pattern elements. The chevron, although probably more defect tolerant since it propagates a stripe domain, could not easily be made in the packing density necessary for this size chip and thus was not considered for the storage area.

As was stated previously, the linewidth and gap dimensions of the earlier chips were determined by the mask and chip processing technology. The desired gap for a 16 μm period was known to be about 1 μm based on scaling from the 28 μm period devices which employed 1.6 micron gaps. Eventually the proper gap (0.8 - 1 μm) and linewidth (2.0 μm) were achieved as chip fabrication technology improved.

Bias margins for the T-bar and chevron patterns can be on the order of 15 percent for the 16 μm period device. This depends, of course, on the device and material parameters. The best demagnetized domain stripwidth (which is approximately equal to the mid bias range bubble diameter) is in the range 3.6 to 3.8 μm for the proper linewidth and gap dimensions. Since the earlier devices had gaps of about 1.1 to 1.3 μm in the fabricated chip, domain stripwidths of 4 to 4.2 μm were used to obtain the desired 10 to 15 percent bias margin in these devices. The larger than optimum stripwidth may also have contributed to the high drive field in the early devices.

Although it is apparent that there is some leeway in the device pattern dimensions and bubble domain diamters, the low drive fields are achieved when the proper dimensions are used. Some additional data on the bias margins versus the chevron period are given in the Item 2 report in connection with the detector optimization task. Permalloy to garnet spacing also must be properly chosen to maintain low drive fields. If the spacing is too great the driving force on the bubble decreases requiring a higher applied in plane field. If the spacing is too small the magnetostatic interaction between the permalloy and the bubble becomes too strong forcing the drive field up to overcome the higher energy barriers to bubble propagation. Spacing can range from 5000 Å to 7000 Å without seriously effecting the drive field. For the devices with the passive replicator component the spacing must be closer to 5000 Å for good replicator operation. A discussion of the device physics concepts which dictate component design and selection is given in Ref 4.

2.3.1.1 Input/Output Branch. - Since the chevron is employed in the stretch type detector and is compatible with the conductor loop type generator and annihilator it was chosen for the section of storage where data input and output is accomplished. The basic criteria followed in this chevron track was to use more than three chevrons in a stack whereever possible but usually not more than five except in the detector or passive replicator. One chevron is actually a pretty poor propagating element. Performance steadily improves as two, three, and four chevrons are used and tends to level off above five (Ref 1). Merging of two tracks is easy to accomplish with chevrons and it is used for the separate generator input track. For the detector the chevron stacks can be expanded abruptly; however, to shrink back to 3 to 5 chevrons after detection (as in the case of the in-line detector) the stacks must only be decreased by one (or at most two) chevrons per period taken from the bottom of the stack. Decreasing from the top will cause some margin reduction especially at the high bias end because the domain strip tends to hang up on the exposed chevron element.

The stacking separation of the chevrons is essentially determined by the processing technology. For the earlier chips the spacing was equal to a linewidth while for the later chips it was less than a linewidth. The tighter packing improves the stripout on the chevron especially in the detector and the passive replicator because of the smoother magnetostatic energy well profile along the stacking axis. The chevron pattern tends to have a larger propagation margin than the T-bar because the chevron can propagate a bubble as well as a stripe domain. However, the limitation of course is in the detector and replicator which require stripe domains for proper operation.

To connect the chevron to the T-bar storage, components called transitions are employed. There are two in each chip at each end of the chevron input/output track. One transition component is essentially the mirror image of the other. Two variations of this component were used in the chip development. Both of them operated satisfactorily. However, the transition element is one of the weaker elements in the design especially at the chevron-to-T-bar port where the stripe propagation is required to convert back to bubble propagation.

2.3.1.2 Corner Components. - For the serial organization both inner and outer type 180 deg corners are needed to accomplish the back and forth path of the storage region. Outer corners are defined here as those in which the bubble circulates in the same direction as the rotating field. Inner corners are those in which the circulation is opposite. The 90 deg corners leading into and out of the chevron composing branch are themselves the transition elements discussed in the last paragraph.

Bent-H type components were used for the outer corners. In the chip development essentially three different bent-H designs were employed. First there was a simple bent-H (having no diagonal bar) with a period equal to the T-bars (Figure 1); next there was a bent-H with a diagonal bar (Figure 2); and lastly there was a simple bent-H having a period about 10 percent larger than the T-bars (Figure 3). The weak point of the first bent H corner (M-1050) is the transition of the bubble from the strong horizontal pole to the bent portion of the H as it approaches the exit area of the corner. The bend in the T weakens the pole at this point. The weakness of this pole is aggravated by the long horizontal bar between the corners. The high drive field (80 Oe) required in the early chips using the simple bent-H was thought to be due totally to the design geometry. Indeed as explained above the geometry did contribute to the high drive field requirement but it appears that the larger than desired linewidths and gaps employed in the early designs were probably the primary cause.

A geometry change was instituted in the M-1061 design in which a diagonal bar was inserted to help the transition of the bubble to the bent-H. Although a significant reduction in drive was observed in this chip (which was primarily the result of the linewidth and gap reductions) a unexpectedly higher drive field was still needed to get the bubble through the bent H corner. Now the weak point was the transition of the bubble from the diagonal bar intercept with the bent-H to the end of the bent H element at the exit port of the corner. The diagonal bar was just too strong a pole. In the third design the diagonal bar was removed and the period of the bent H was extended to provide some increased pole strength and again the linewidth and gap dimensions were reduced. The final bent-H design (M-1065 through M-1067B) seems to have adequate performance although as with all corners, it is somewhat more sensitive to geometry variations and bit-bit interactions than is the T-bar storage element.

For the inner corner two different component designs were employed in the chip development. Based on a study of various corners performed before this program (Ref 5) an X-bar type corner was chosen for the earlier chip designs M-1049 and M-1050. Again because of the large linewidth and gap dimensions of these chips the performance was not satisfactory, and so in the next chip design, M-1061, the inner corner design was changed (along with the linewidth and gap). This time a T-X design was used since it was felt that more poles would help the bubble travel around the 180 deg turn more smoothly. This corner has performed at least as well as the other component designs in the chip and is used in the final chip design (M-1067B) with some slight modification required by flash composition of the Mann 3000 pattern generator (Section 5).

2.3.1.3 Asynchronous Operation. - This mode is required by the system so that data can be transmitted at variable data rates. Although the bubble memory chip is capable of operating at variable speeds the asynchronous requirement is achieved by periodically interrupting bubble propagation which takes place at the intrinsic field rate of 150 kHz. This requires that the chip start and stop in a systematic manner so that data reliability is maintained. There are two requisites to effect reliable start-stop operation. First the in-plane field must build up to its operating value before field rotation for propagation is commenced. Beginning to rotate the field below or too close to its minimum value may cause errors. Then to stop the device the rotation of the field must be halted and decayed to zero with no more than a 1 Oe overshoot. Too large an overshoot may cause data scrambling. Secondly, the bubble domain stopping positions on the propagation pattern must be stable during the time the drive field is off or be stabilized by a small, static in-plane holding field.

The second requisite was the more important one in the chip development task where the best pattern designs and orientations had to be selected so that operation in the asynchronous mode would be reliable. Much of the data and design principles used in this selection are contained in Refs 6 and 7 where start-stop on various propagation circuits was studied as a function of start-stop direction and inplane holding field and direction. To illustrate the problem associated with the asynchronous mode, start-stop results on an isolated T-bar pattern and a 20K bit device similar to the M-1061 100K bit chip design are shown in Figure 6. For the T-bar pattern the best start-stop direction is parallel to the bars of the pattern. One possible reason for this is that it allows only one bubble to rest on each individual pattern element thus minimizing bubble-bubble permalloy mediated interaction. Note also that a small holding field in the start-stop direction will improve the margin to some asymtotic value (i.e., the continuous mode margin) while an opposite (or unfavorable) holding field will result in severe degradation of the margin. To compensate for unfavorable fields generated from anomalies in the packaging or from stray fields and the like, a small holding field is generally required for reliable start-stop operation.

After devices M-1049 and M-1050 the start-stop direction was chosen as to be in the direction of propragation in the chevron input/output track. The T-bar storage track was reoriented accordingly for the later devices. The weakest point for start-stop on the chevrons is at the apex location, however, with a suitable holding field and drive field its operation also is adequate. When the passive replicator was included there was some question about its start-stop performance; however, the data included in the Item 2 report on the device M-1064 demonstrates the suitability of this component in start-stop operation.

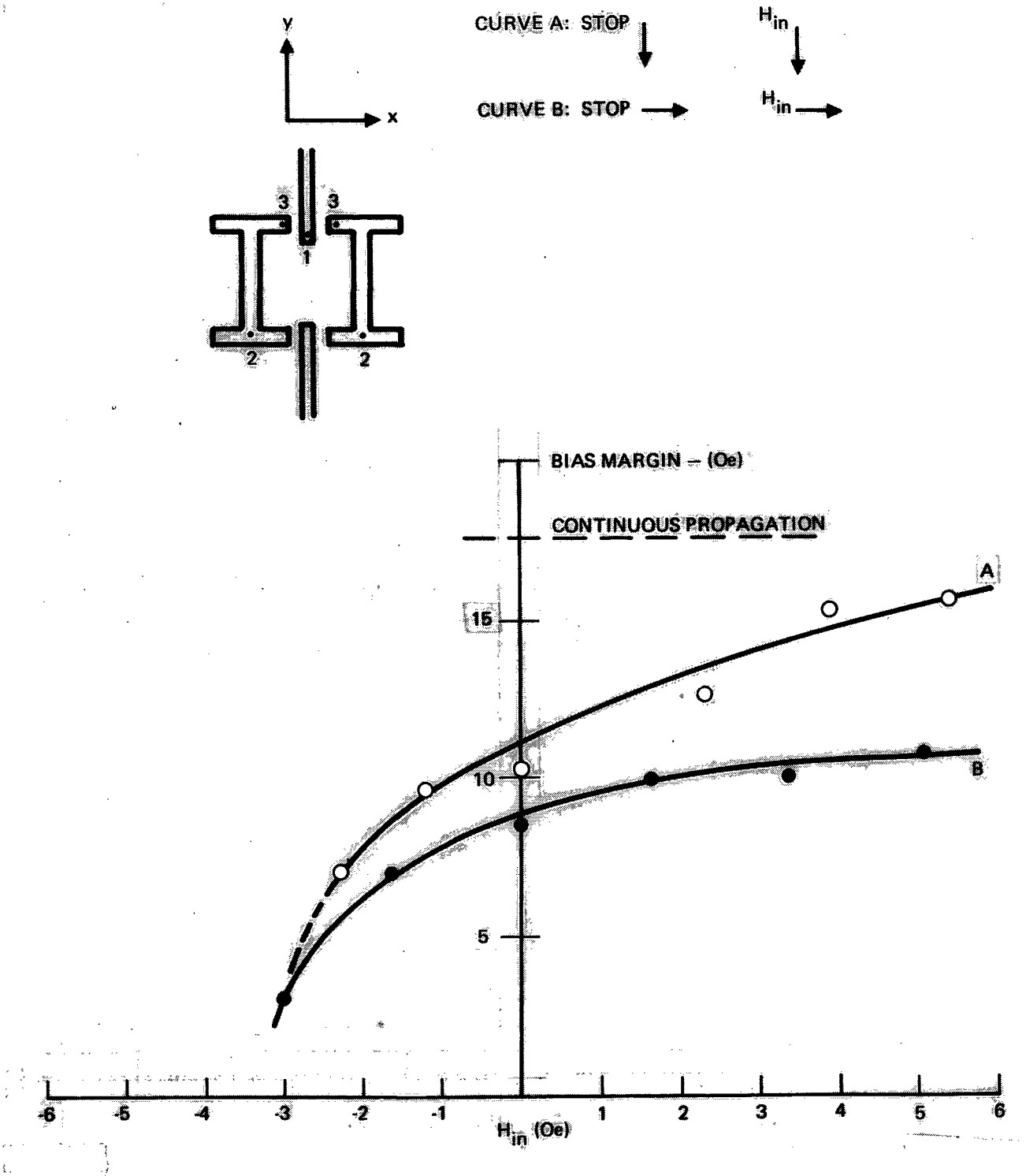

Figure 6. Start/Stop Propagation Margins vs In-Plane Holding Field for a T-Bar Pattern (Ref 7)

2.3.2 Detector. - To simplify the device fabrication on this program a single level thick permalloy chevron stretcher detector was employed. The basic design employed is the zig-zag interconnect geometry which has given adequate detector performance. A detector study which investigated the magnetoresistive switching process in regard to drive field and detector geometry is given in the Item 2 report. Besides giving some insight into detector operation the study concluded that the zig-zag design was as good as any other single level design and that the chevron period should be longer than 16 μm (~19 μm) for the best combination of detector operation and propagation in the chevron track.

The two areas of primary concern to detection are the signal to noise level and the first bit detection requirement for asynchronous operation. Each area will be covered separately in the following paragraphs.

2.3.2.1 Signal to Noise and Error Rate. - The program goal for detection was stated in terms of the signal to noise parameter as 15 dB. Usually when the detector is evaluated for performance the error rate is measured as a function of detector threshold. A typical error rate curve is shown for the M-1061 100K bit device in Figure 49. If it is assumed that the noise at the detector is primarily due to the magneto-resistive switching and is random and that the noise distribution for the zero and one signal are about the same the signal to noise can be written as (Ref 8).

$$S/N = 20 \log_{10}\left(\frac{V_{th}}{2\sigma}\right)$$

where σ is the standard deviation for the noise distribution and V_{th} is the threshold window at an error rate of 0.5. For the detector in Figure 49 the S/N = 13 dB which, although somewhat less than the goal, appears to be adequate based on results of actual detector use. From the figure the detection soft error rate will probably be on the order of 10^{-12} errors/bit or less.

The first device developed employed only 30 chevron elements which generated only about 100 μv/ma signal sensitivity. Thus, in the later designs the detector stretch was increased to 100 chevrons to increase the signal level but yet be consistent with the requirement of first bit detection. As indicated in Figure 60 the signal sensitivity is at least 0.3mV/ma at 60°C which surpasses the program goal. Figure 57 illustrates the good matching between chips and the suitable window over temperature.

2.3.2.2 First Bit Detection. - One of the more difficult problems in the development of a suitable device was to ensure that the bubble domain which stopped just before the sense element could be reliably detected when the chip was restarted (in the asynchronous mode). The device design features that were affected were primarily the length of stretch of the detector and its orientation to the start/stop direction of the rotating field. First bit detection seemed to be no problem in device M-1061 which employed a 100 element stretch, in-line detector. However, the system requirement for coincident read/write/erase motivated the change to a passive replicator and a guardrail detector. The most convenient placement of this detector was in a horizontal orientation as was the case for device M-1065 (Figure 4). This orientation was suitable for start/stop operation (Ref 6). However, it was not known if the domain located in the chevron gap at the entrance of the detector could be stretched to full length or near full length in the half cycle between startup and detection.

Before device M-1065 was available some measurements were made on existing devices to determine whether stripout could be expected for the horizontal orientation. Figure 7 shows the results for start/stop along the gap of a 36 element stretch detector on YSmLaGaIG material where the bias field is near the center of the propagation margin. The test coil used for these measurement had a relatively slow rise time ($\tau \approx 6\mu$sec) because it was a special open structure to allow visual measurement of the domain stretch by the laser strobe technique (Ref 1). The curves show the time dependence and spatial relationship of the drive current components Ix and Iy. The vertical position of the numerals represents the length of domain stretch observed at that time interval. The value of the numeral represents the number of times a domain was observed to have that length. Ten measurements or observations were made at each time interval. It can be seen that domain stretching does not actually commence until the field starts to rotate and even then it is very erratic and incomplete. It appears from this data that even if a long precharge time (holding the drive stationary at peak value for a number of cycles) were used the domain would still not stripout. Since at higher bias the results will be even worse, it seems that start/stop antiparallel to the chevron apex direction is not satisfactory for first bit detection.

These measurements were repeated for the case where the start/stop direction is parallel to the propagation direction in the chevrons as it was for device 1061. Figure 8 shows the results of these measurements in the high bias region of the propagation margin. In contrast to the previous case the domains stripped out in less than 1.7τ (10 μsec). Note that after about time 0.7τ the domain stripout velocity very quickly reaches its peak velocity of 7.5 chevron elements per μsec (~32 m/sec). Some collapse of the stripe occurs as it passes the apex of the chevron after the field begins to rotate, however, it may just indicate that the bias field used in the measurement is a little too high to support complete stripout in the chevrons. At a slightly lower bias field this effect would not occur.

In actual measurement (Figure 51) this detector was operated satisfactorily in first bit detection with only a one cycle precharge; thus maximum data rates of about 135K bytes/sec would be possible at 150K Hz asynchronous. For the Ga substituted material and the 150K Hz frequency it would appear that for reliable first bit detection down to -10°C it would be best to design for at least a one cycle precharge. However, it does not seem that more than two cycle precharge would be necessary. The best start/stop direction based on the laser camera stripout measurements is parallel to the propagation direction in the detector chevrons with the first bit to be detected stopping on the chevron column just before the detector chevron stack.

Margin data taken on the M-1067 design shown in Figure 51 include first bit detection under 8-bit gated asynchronous operation. The margins are good indicating that first bit detection is good for this device. Very little statistical data has been taken with first bit detection at this time; however, it is expected that the vertical detector orientation will prove to be the more reliable design especially with the straight feedthrough design (Figure 5). Commercial modules employing eight chips of the 1067 design have been operated successfully over 0°C to 50°C in the asynchronous mode leading additional confidence to the expected performance of this design in multichip data recorder modules.

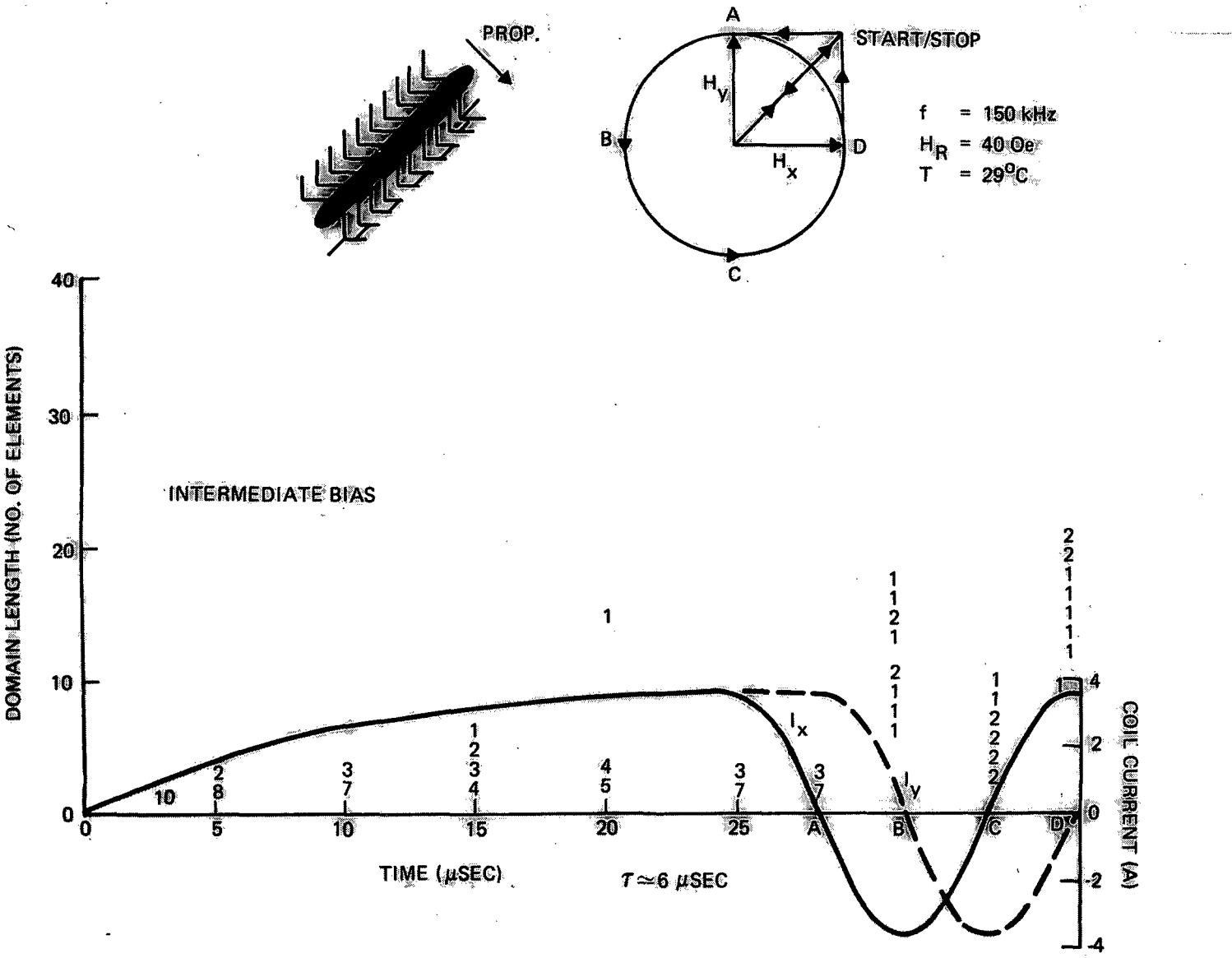

Figure 7. Domain Stripout for Start/Stop in the Chevron Gap

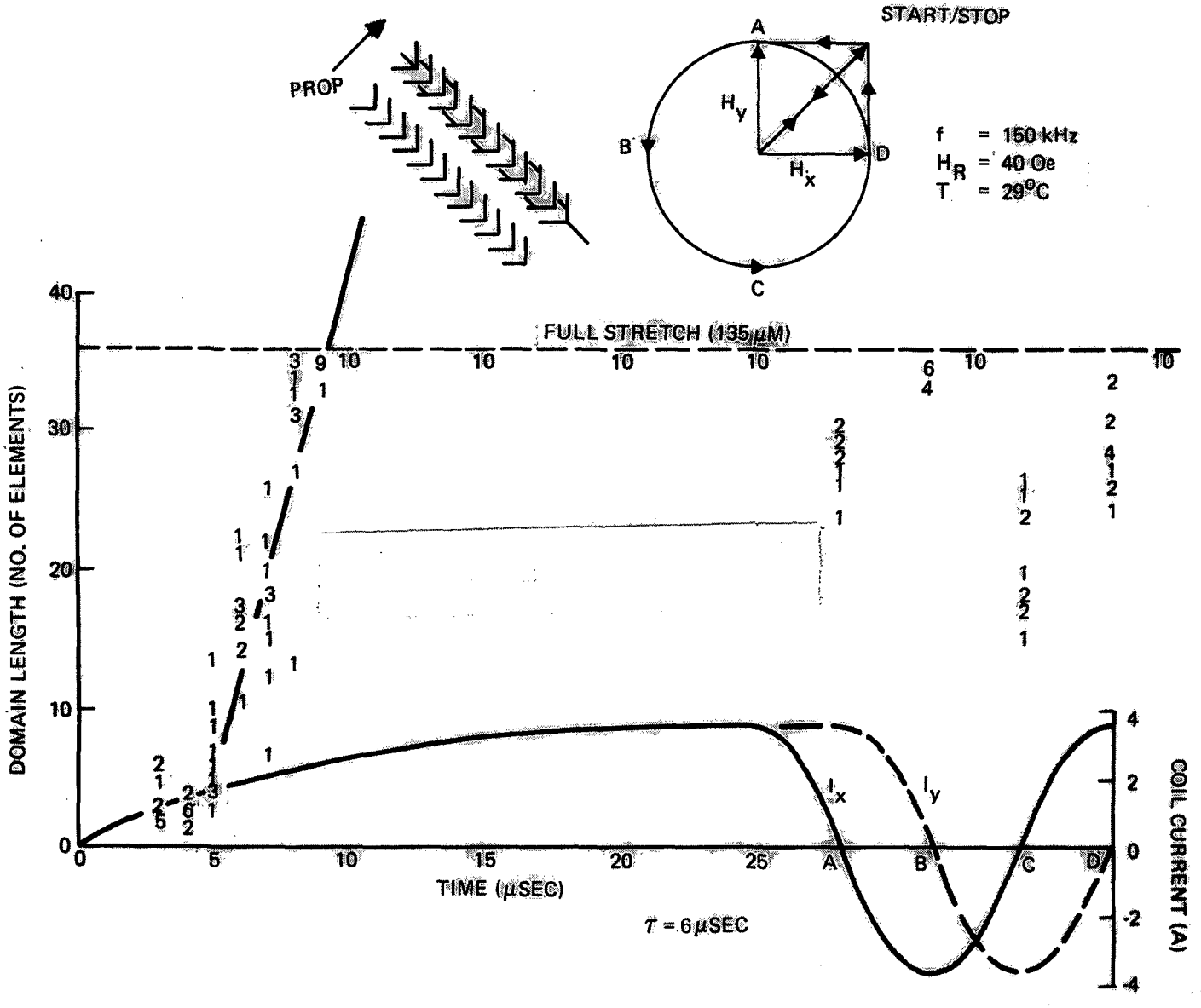

Figure 8. Domain Stripout for Start/Stop in the Chevron Propagation Direction

2.3.3 Passive Replicator. - The majority of the effort to develop this component for the FIFO chip was done in the Item 2 portion of this program (Ref 1) and is covered in detail that report. The best design evaluated in this study was employed in the final version of the 100K bit chip (Figure 4). Some characterization data on this component obtained through bias field interrupt measurements (Ref 9) on M-1067 chips is given in Figure 53. The passive replicator component is basically the limiting component of the device. At high bias its failure mode is due to incomplete strip out which can result in a hard error if the domain propagates out to the detector without replicating. At low bias the failure mode is due to a failure of the stripe domain to be cut. Cutting is accomplished by the local permalloy fields at the end of the cutter bar which is a period long bar (two chevrons in adjacent columns connected together with an extension on the downstream end) at the center of the replicator component. Reliable operation of the component usually requires higher drive fields than the other components to accomplish complete stretching and cutting of the stripe. The stretching and cutting process can be aided indirectly by employing a closer permalloy to garnet spacing. For devices utilizing this passive replication design the spacing is nominally made 5000Å rather than the 6000Å to 7000Å that would normally be used for this period device. The closer spacing does not seriously effect the other propagation characteristics, however it does present some problems with step coverage over the conductor.

2.3.4 Generator. - The most common technique used for generation of bubbles with diameters of 4 μm or larger is the nucleate generator which consists of a simple conductor loop positioned on the permalloy track. Because of the high current densities required (10^6 amps/cm^2) nucleate generators are normally not used for smaller bubble devices. In the two level type devices the generator as well as the annihilator are fabricated in a conductor-first process sequence where a highly conductive metal (such as Aℓ-Cu) is used. (see Section 3.) Reliable generation from -10°C to +60°C requires a pulse of about 200 ma with a 0.2 μs duration. For the M-1067 design the generator will operate satisfactorily with the pulse located between 140 deg and 235 deg. Although individual devices may have wider phase margins the values indicated are suitable to allow operation of matched chips over the temperature range -10°C to +60°C. The phasing as well as the pulsewidth required are insensitive to temperature; however, the pulse amplitude required decreases with temperature. A single value of generator pulse amplitude can be used over the temperature with its value being determined by the low temperature requirement.

The generator loops in all the devices of this program are located on an adjacent chevron track which merges with the storage track. The loop is not placed right on the storage track because of the possibility of reduced phase margin as a result of incoming or outgoing bubbles being annihilated on the outside edges of the loop where an unfavorable field is generated. With improvements in generator design the plase margin has been made quite wide (>180 deg); however, the generator loop has never been placed back on the storage track. The merging design seems to work quite satisfactorily.

A more important consideration was the failure mode in which multiple domains could be generated. This occurred frequently in the generator loops which completely covered the entire height of the chevron stack (Figure 1). In operation either two bubbles were generated, one at the top of the loop and the other at the bottom, or the nucleated stripe domain somehow stretched between two periods and then split,

forming two bubbles. In any case this failure reduced the phase margin for generation, especially at the higher temperatures where the wall energy is lower. This failure mode was virtually eliminated by shortening the generator loop so that it only covered one of the five chevrons in the propagation track (Figures 2 and 3). The position of the generator loop was maintained at the center of the chevron gap in all devices. Although the phase margin is relatively insensitive to positioning, some shift in the center margin will occur with misalignment.

2.3.5 Annihilator. - The annihilator component is also a conductor loop but it is positioned directly on the chevron storage track. The current in this loop is opposite to that of the generator so that the magnetic field generated aids the bias field raising the region under the loop above the bubble collapse point. To annihilate over the operating temperature range requires a current of approximately 130 mA, and 0.2 μs duration. Too high a current will result in a failure mode in which bubbles are generated on the outer edges of the annihilator (see Figure 54b).

The alignment tolerance of the annihilator is somewhat critical since the phase margin is about 45 deg. Early annihilator loops (M-1061) were centered on the chevron gap similar to the generator positioning. Laser strobe measurements of chevron propagation (Ref 10) revealed that the bubble domain spends a small amount of time in the gap region, traveling very rapidly from one chevron to the next. Thus the M-1061 annihilator had a relatively narrow phase margin (45 deg) which caused some difficulty in finding a number of chips that would operate well since small shifts in the loop position caused corresponding shifts in the center of the phase margin. The laser strobe measurement also showed that the domain pauses for a period of time at just about the center of each leg of the chevron. An increase of phase margin to better than 90 deg was obtained by moving the center of the annihilator loop closer to this location (Figure 3). The M-1050 device, although it had a centered annihilator, had a good phase margin because of the much wider loop which effectively placed one side of the loop downstream.

The annihilator pulse can be located between 150 deg and 210 deg; however the earlier phasing edge appears to be somewhat more sensitive to alignment variations and some other unknown factors and therefore it appears to be more appropriate to locate it between 195 deg and 210 deg. Again phasing and pulsewidth appear to be insensitive to temperature. Also the pulse amplitude required decreases with temperature and since the annihilator has a minimum/maximum limitation the use of a fixed annihilator amplitude over the entire temperature range may not be possible. When considering a small sample of devices an adequate amplitude margin appears to exist; however, for a much larger sample the amplitude margin may become very narrow. In this case it would be necessary to track the annihilator pulse amplitude with the temperature variation.

3. DEVICE FABRICATION

The basic operations in two mask level bubble chip processing are shown in Figure 9. During the course of the device fabrication runs made on this program the sources of yield loss associated with the various device processing operations were determined. Process reviews were performed at the conclusion of each device fabrication run as a part of an overall Critical Design Review, and appropriate process modifications were made to improve the device yield. The detailed discussions of the interactions and tradeoffs between device design, processing, performance and yield are contained in Sections 2, 5, 6 and 7. The bulk of the information on device yield performance improvement through process evaluation and modification is presented in Section 6. Consequently, this section is devoted primarily to a general description of the basic process capabilities and procedures utilized during the course of the program with a minimal amount of detail on the process evaluation and the motivation for modifications.

All operations are performed in a Class 30,000 clean room supplemented with laminar flow hoods.

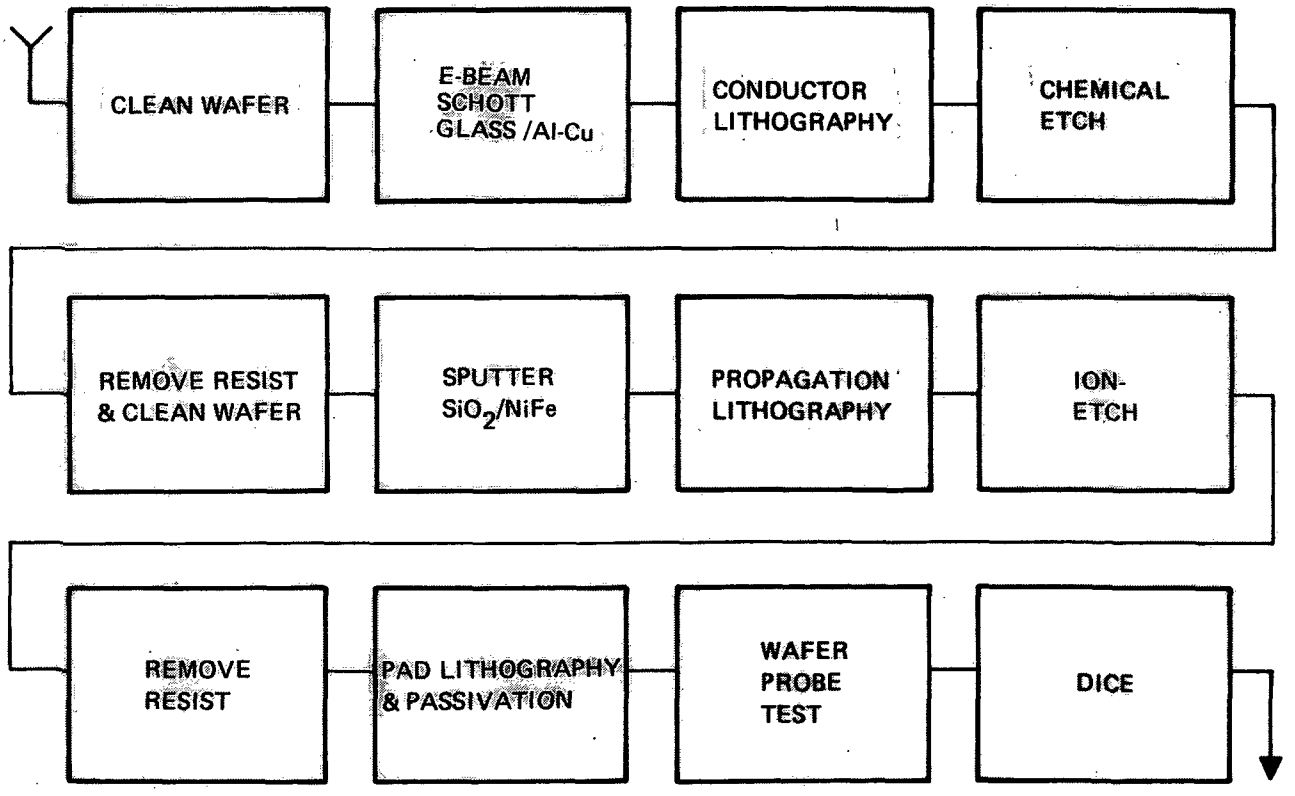

Figure 9. Bubble Device Processing

3.1 Wafer Cleaning

The tediousness of initially cleaning each wafer individually has been eliminated by using a cartridge to cartridge automated wafer scrubber without sacrificing the quality of the cleaning operation compared to manual cleaning. The cleaning operation consists of loading each wafer on a vacuum chuck which is rotated as various solutions are dispensed sequentially on the wafer. Scrubbing the wafers is accomplished using a mohair brush and a detergent scrubbing solution, followed by an alkaline rinse, deionized water rinse, and spin blow dry. The wafers are then reloaded into a separate cartridge which is placed in a clean cartridge container for transportation to the next work station. A laminar flow hood maintains ambient particle count at a level better than class 100.

This cleaning operation is modified when the wafers are processed prior to SiO_2/NiFe deposition since both the alkaline rinse and mohair brush can cause damage to the conductor layer. The cleaning operation instead consists of acetone rinse to remove resist, individual swabbing with a liquid detergent without rotating the wafer, rinse, and spin dry.

3.2 Barrier Layer and Conductor Deposition

Initially, a sputter-deposited layer of SiO_2 preceeded an electron beam evaporated layer of Aℓ-Cu in order to minimize stress gradients produced in the LPE bubble film by direct contact with the conductor layer. It also alleviated another effect (Ref. 11) which manifests itself in leaving a pattern image in wafers which have been processed and subsequently stripped-back for reprocessing. This effect has been ascribed to gallium redistribution resulting from oxygen gettering at the wafer/metal interface. The two separate processing steps were subsequently combined into one operation by using Schott glass for the barrier layer which was electron beam deposited during the same pumpdown as the Aℓ-Cu deposition. In addition, the tooling from the baseplate through the planetary fixturing was redesigned. A four pocket, 270 deg E-gun is now used as a source, and a planetary fixture with quartz lamp substrate heating has been installed which is capable of handling 25-2 in. wafers in a single pumpdown.

3.2.1 Schott Glass Barrier Layer. - It was reported in the process review at NASA on 4/1/75 (Ref. 12) that the sputtered SiO_2 barrier layer was deposited at an average thickness of 1100Å with a mean square deviation of 335Å during the first yield run. This result compared with an objective of 1000Å ±200Å. As a result of switching to evaporated Schott glass the following benefits were derived:

1. Both barrier layer and conductor could be deposited in a single pumpdown.
2. Up to 25-2 in. wafers could be coated at a time.
3. Deposition time was also reduced due to the higher evaporation rate versus sputtering rate (225Å/min versus 50Å/min).
4. Excellent adhesion is obtained by proper wafer cleaning and prebake prior to deposition.

5. Film thickness is now 800 ±100Å on ≥90 percent of the runs as measured on a Dektak (Ref. 13) thickness profilometer. The use of a cone shutter has also proved useful in reliably establishing deposition rates prior to film deposition. When the desired thickness is not achieved the cause is traceable to drift in the thickness monitor.

3.2.2 Aℓ-Cu Conductor Deposition. - The procedure for depositing Aℓ-Cu has not changed since the program start. The target thickness of 4250 ±150Å is routinely met.

One pocket of the four hearth E-beam gun is loaded with an 80-20 Aℓ-Cu charge, which has been precleaned, in order to achieve a film composition of 96-4 wt percent Aℓ-Cu using a deposition rate of 400A/min. Sheet resistance is measured on a four point probe and is maintained in the range from $0.45 \leq \rho_s \leq 0.72$. Adhesion to the Schott glass has not been a problem.

3.3 Insulator Layer and Permalloy Deposition

Both SiO_2 insulator layer and NiFe film depositions are made during a single pumpdown by RF sputtering in an 8 in. MRC (Ref. 14) system equipped with a multiple target and multiple substrate platen capability. Although both depositions are performed in a single pumpdown, this operation remains one which requires relatively long deposition times due primarily to the time required to deposit the SiO_2 layer. Alternatives which have been investigated, however, have not proved as process compatible as sputter-deposited SiO_2. Major modifications of the equipment which have resulted in improved run-to-run uniformity are the use of ethylene glycol cooling and incorporation of a thickness monitor.

3.3.1 SiO_2 Insulator Layer. - Previously it was reported (Ref. 12) that SiO_2 thickness was the most difficult to reproduce. The figures reported showed an average thickness of 7100 ±640Å MSD (mean standard deviation) compared with a goal of 7000 ±350Å. Most recent figures show a goal of 4200 ±350Å being attained in 80 percent of the runs. A thickness of monitor has been mounted adjacent to the substrate platen and serves as a monitor of film thickness. Previously, targeted film thickness was estimated using input power (deposition rate) and time as parameters. Adhesion of SiO_2 to the Aℓ-Cu conductor layer and step coverage have not been a problem.

The relatively slow deposition rate of SiO_2; 50Å/minute, is necessary due to constraints on the maximum allowable substrate temperature reached during deposition. If the input power is too high the substrate temperature will increase to 300°C and cause hillock formation in the Aℓ-Cu conductors. At even higher power inputs cases have been observed where the Aℓ-Cu has actually melted. The slower deposition rate also results in better thickness control since higher deposition rates cause excessive heating of the SiO_2 target which results in erratic deposition rates and interaction with the thickness monitor.

3.3.2 Permalloy Deposition. - Thickness control and magnetic properties of the sputtered NiFe file are now routinely achieved. In the first yield run (See Chapter 6) it was reported that the target thickness of 4000Å was being achieved on the average but the mean deviation (±560Å) exceeded the objective of ±350Å.

The present thickness control achieved routinely is 3250 ±250 Å. Other parameters of the NiFe film which are monitored and maintained are:

Coercive Force (H_c) ≤ 1.5 Oe

Saturation Magnetization ($4\ M_s$) ≥ 9K Gauss

Magnetoresistance ($\Delta\rho/\rho$) ≥ 2.5 percent

A major cause for this improvement is related to the use of ethylene glycol coolant. It has been shown (Ref. 15) that low target impedence keeps RF heating of the target low and as a result improves reproducibility. Erratic target impedences have resulted from the use of water coolant with variable conductivity. A second factor which has resulted in improved magnetic properties is the use of higher deposition rates (high power input) of 300Å/min. This improvement is attributable to the higher substrate temperature attained as a result of higher input power.

A lot of 8 wafers is handled in a single pumpdown by placing 4 wafers on two 8 in. dia copper platens. Three monitor slides are included in the center of each platen which are subsequently used to measure film thicknesses and magnetic properties. The uniformity over the four wafers is better than ±10 percent for both NiFe and SiO_2 deposits. Uniformity over a single wafer is better than ±5 percent.

The measurement of H_c and $4\pi M_s$ was made on a conventional hysteresis loop tracer. Magnetoresistance is measured in the following manner. One of the monitor slices is a rectangular silicon strip, 0.85 in. x 0.08 in., which is placed on a four point probe and subjected to a small dc longitudinal field and a transverse ac field supplied by orthogonal Helmholtz coils. The corresponding change in ρ is measured on an oscilloscope CRT by measuring the corresponding ΔV picked up by the voltage output from the four point probe. Although the acceptable lower limit is 2.5 percent, values as large as 3.9 percent have been attained.

The 8 in. Ni-Fe target used consists of 81.0 wt percent nickel. The film composition has correlated with the target composition within experimental accuracy. Prior to deposition a shutter is placed between the target and substrate platen and the target is backsputtered to guarantee a clean source surface before initiating deposition.

3.4 Photolithography and Pattern Definition

The photoresist used for all process steps is AZ 1350J (Ref. 16) which is handled by an automatic photoresist spinner and developer manufactured by III Corp. (Ref. 17). Vacuum pickup tools are used to assist in wafer handling. Alignment and exposures are performed on Kasper 2001 aligners (Ref. 18). All operations are made under laminar flow hoods. Wet chemical etching is used to pattern the Al-Cu conductors and remove sputtered SiO_2 from the aluminum bonding pads. Ion-beam etching is used to define the permalloy pattern.

3.4.1 Photolithography. - Both contact and projection lithography were investigated, a Kasper 4:1 aligner being used for projection. It was determined during the course of the program (Ref 12) that contact lithography could be pursued to meet the performance and cost goals. The 4:1 aligner was incapable of resolving 1 μm over the area of a 2x2 array of 100K bit devices which was necessary to generate a 6x6 array using the 3x3 step-and-repeat capability of the machine. An example of the lithography obtained, using a black chrome 4X mask, at the corners and center of a

100K bit pattern is shown in Figure 10. Considerable blooming of the bars is observed at the gaps of the T-bar elements as well as considerable rounding at the end of a bar The 4X black chrome mask from which this print was made is shown in Figure 11. Although lack of resolution was the main reason for abandoning the projection approach, other factors contributed to the difficulty in operating the machine. Had they been resolved it may have been possible to achieve the required resolution. These factors may be summarized as follows:

1. Optimum alignment focus is not the same as the optimum exposure focus - adjustments must be made after alignment due to the limited depth of focus (4μm).

2. Alignment light source illuminates wafer at all times which requires shuttering or improved UV filtering.

3. Need to use thinner photoresist than used in contact printing to get improved resolution - this impacts processing, e.g. ion milling.

4. A modification was needed to provide better illumination of alignment marks.

Iron oxide and emulsion 4X masks were also evaluated on the 4:1 projection aligner without any significant differences being observed. In view of the continued problems with the projection aligner and the encouraging results using contact lithography, all subsequent device processing was performed using contact lithography for the propagation layer and either contact or proximity printing for the conductor layer and oxide removal from the bonding pads.

The importance of intimate contact between mask and wafer is shown in Figure 12. By properly adjusting the pressure it is possible to reproducibly obtain the patterns shown in (a) provided the wafers are within flatness specification. A gradual deterioration of gap width, linewidth, and resist profile is observed in (b) - (d) as mask-to-wafer contact deteriorates. While the image in (b) is visibly degraded, the ion milled image will likely be as good as the ion milled image from (a). The photoresist image in (c) might yield passable device structures but the image in (d) would definitely lead to poor gap definition and shorted elements.

3.4.2 Pattern Definition. - Three pattern definition operations are performed, two being wet chemical etching to define the conductor pattern and open the bonding pads, and one being ion-beam etching to define the permalloy propagation pattern.

The chemical etchant used to define the conductor patterns is a 20:4:1 phosphoric acid:acetic acid:nitric acid etch at 50^{o}C. Sloped wall profiles, shown in Figure 13, are achieved by etching the aluminum-copper without postbaking the photoresist. The importance of the sloped walls is shown in Figure 14 which shows a permalloy element crossing over the conductor. When the wall slope is in the vicinity of 45 deg the permalloy step coverage is smooth and uniform. When the slope is nearly vertical step coverage is poor resulting in discontinuities in the permalloy. This problem and its impact on device performance has been described previously. (Ref 19.)

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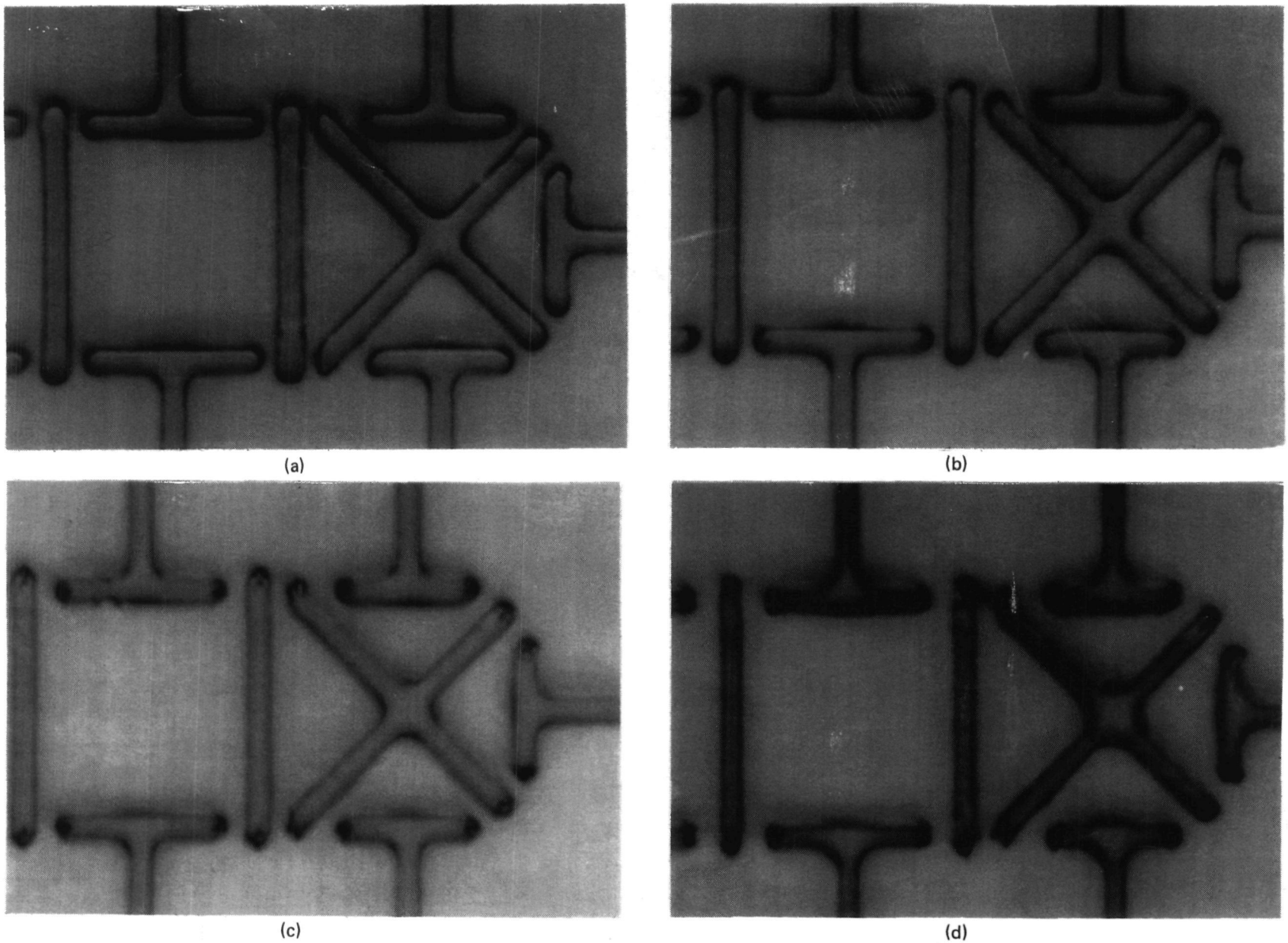

Figure 12. Contact Printed 1350J Photoresist Images Showing the Effect of Degraded Mask-wafer Contact. (The good contact in (a) progressively degrades from (b) to (d). The gap widths are approximately 0.8 μm)

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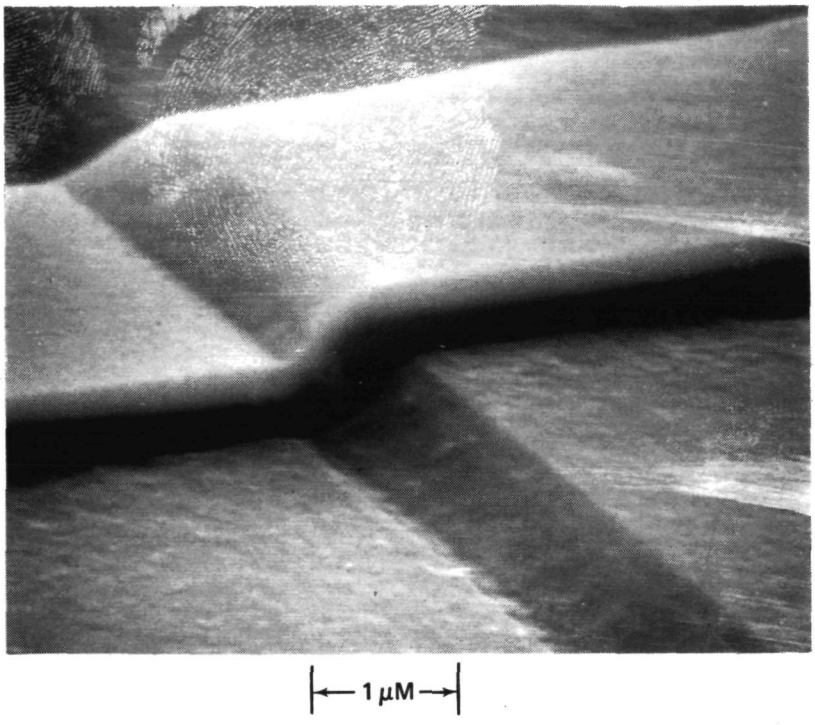

Figure 14. Step Coverage of Permalloy Element Over Aℓ-Cu Conductor After Removal of Resist

The SiO_2 on the bonding pads is removed with buffered HF after passivation of the device with a 2.5 μm layer of AZ1350J. Complete removal of the SiO_2 is verified by a continuity check of the conductor loops with gold wire probes. Complete removal of SiO_2 is necessary to achieve good ultrasonic bonding of the Aℓ ribbon, used for electrical connection of the chip to the carrier board metallization.

The permalloy pattern is defined by ion-beam etching using a Veeco Microetch (Ref 20) system which has the capability of handling six 2 in. wafers/pumpdown. Each wafer is mounted on an individual pedestal which is indexed into milling position on a "lazy-Susan" type fixture. A thermal transfer agent is used between the wafer and the pedestal to promote removal of heat during the operation. During a typical operation the substrates will reach 200°C when milled at a rate of 250 Å/min.

Typical wall profiles of the patterned permalloy are shown in Figure 15. A 1.5 μm thick layer of AZ1350J is used to provide adequate masking of the patterned area since with ion-beam etching the resist, as well as the permalloy, is eroded during etching. This technique provides a faithful reproduction of the resist pattern in the permalloy with negligible undercutting.

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3.5 Wafer Dicing

Wafers were initially diced using a wire saw with 8 mil diameter wire impregnated with 45 μm diamond grit. A protective coating of KTI laser scribe material was applied prior to dicing. The typical kerf was 12 mils. Since the cutting time for one cut across the wafer was up to 15 min, depending on wire wear, wire saw dicing was a time consuming process. Furthermore, it was a dirty process resulting in low device yield.

As a second attempt at wafer dicing, the use of a high speed "super saw" was proposed. This saw, however, could not be used for garnet dicing due to the fragile nature of the thin cutting blades. Typically, the blades disintegrated after several cuts across the wafer. The usual result was wafer damage with resultant yield loss.

Presently, wafers are diced using a laser scribe and break technique. Using a CO_2 laser scriber, Coherent Radiation Model 42 (Ref. 21), kerf widths of 5-6 mils are obtained. The normal scribe time for a 2 in. diameter wafer into 0.25 in. squares (100K bit die) is five minutes. More importantly, this dicing method has a high process yield, approximately 90 percent after all handling. The initial step in this process is the inspection of the wafers to identify any damage, such as a chip at the edge of the wafer, which may need to be taken into consideration when scribing in order to prevent unnecessary irregular wafer cracking. The wafers are then cleaned and coated with KTI laser scribe material #111. The laser scribe is cured at 115°C for 15 min. The wafers are backside scribed using the CO_2 laser scriber. The depth of cut is approximately 50 percent of the wafer thickness.

Once the wafers have been laser scribed die are separated from the wafer by a hand break method. The wafers are placed scribe lines down on a clean silicone rubber pad and covered with a clean mylar sheet. An appropriately sized glass rod is then placed on the mylar sheet above a scribe line and pressure is applied until the wafer breaks along the scribe line. This process is continued until all dice are separated. Dice are then carefully stored in clean chip carrier boxes until final cleaning just prior to die mounting for acceptance testing.

The final cleaning operation consists of a gentle agitation for 10 sec in xylene followed by a similar isopropyl alchohol rinse. The die are then spray cleaned using Cobehn (Ref. 22) cleaning solution. Cleaned dice are dried with N_2.

3.6 Summary

The device processing sequence and target thicknesses are summarized in Table 4.

TABLE 4. PROCESSING SEQUENCE

Step No.	Thickness (A)	Material/Function	Technique
1	800	Schott Glass barrier layer	E-beam
2	4,250	AlCu conductor	E-beam
3	15,000	AZ1350J Conductor Pattern	Standard Photolithography
4	-	Chemical Etch AlCu	Immersion
5	4,200	SiO_2 insulator	RF Sputter
6	3,250	Permalloy Propagate	RF Sputter
7	15,000	AZ 1350J Propagate Pattern	Standard Photolithography
8	-	Ion-etch Permalloy	VEECO Micro-etch
9	25,000	AZ 1350J Oxide Pattern and Passivation	Standard Photolithography
10	-	Chemical etch SiO_2	Immersion
11	-	Wafer Probe	-
12	-	Dice	Laser scribe and break

4. CHIP PACKAGE/ASSEMBLY TECHNOLOGY

The bubble memory device package/assembly requirements are similar to those of the microelectronic device technology. Much of the assembly materials, assembly techniques and package materials are of the type used in semiconductor package/assembly technology. Some of the differences which are unique to the bubble device technology lie in the necessity for tight controls on the chip surface planarity, chip electrical connection (wirebonds) to minimize $d\phi/dt$ pickup, rectilinear chip alignment tolerances and the need to construct a package which does not distort the dc magnetic bias field or the high frequency rotating drive field. In addition, the package/assembly and design requirements must meet the normal criteria of minimized volume, weight and power requirements while performing within the environmental and ambient requirements of an airborne or spaceborne microelectronic system.

Although this program did not require a specific package design the chip design, fabrication, and package/assembly techniques had to be such that the chip could be used, eventually, in such a rugged environment. The contract called for a single chip package design and an assembly technique in which the chip could demonstrate the capability to withstand specified environmental stresses. The environmental tests were performed only to demonstrate the potential suitability of the packaged chip in a space mission environment. The objectives of these tests were to detect potential failure modes and not to serve as a device acceptance criteria.

Accordingly the contract called for the single chip package to be subjected to the following tests:

1. Thermal Tests

   a. Perform a temperature cycle test consisting of 15 cycles of: (1) 5 min. at $T_A \leq 0°C$, (2) 5 min at $T_A = 25°C$, and (3) 5 min at $T_A = 150°C \pm 5°C$ with transfer times to be less than one minute.

   b. Perform a thermal shock test consisting of 15 cycles of 5 min at $150^{o}C$ $\pm 5°C$ and 5 min at 0°C with transfer time between temperature limits to be less than 5 sec.

2. Mechanical Tests

   a. Perform a mechanical shock test consisting of 3000g for 0.5 msec.

   b. Perform a mechanical vibration test at 30g, 20-2000 Hz along 3 axes with devices mounted rigidly such that an amplification factor of 1 can be assumed.

   c. Perform a centrifuge test at 2000g, 5000g and 10000g each on 3 axes.

All failures to these tests were to be analyzed to determine cause and remedial action, if warranted, to be recommended to NASA.

These tests were primarily designed to evaluate the techniques of die bonding to package surface and the wire bonding connection between the die and the package metallization. A wire bond strength test was initiated to determine the integrity of the wire bond connection between chip and package. A preliminary study of bonding parameters was performed using 0.001 in. diameter gold wire and a 0.001 by 0.003 in. gold ribbon bonding to two types of device bonding pad material and one chip carrier bonding surface. The purpose of the bonding schedule development tests are to determine that combination of assembly parameters (bond temperature, bond force and pulse time) which will result in a 40 to 50 percent deformation of the bond material and provide a bond configuration which will survive the wire pull strength test. Figure 16 shows a typical bond parameter spectrum test. Each of the points plotted in Figure 16 represents ~10 to 15 bonds. The heat pulse width and height are varied to produce bonds whose bond site dimensions vary from < 1.4 to $\gtrsim 1.5$ times the visible width of the bond wire. These bonds are then subjected to pull tests with the criteria that when pulled, the yield strength of the bond wire must be the limiting factor in the strength of the connection. The results shows a wide acceptable range of bonding parameters for all bond material to bond surface combinations. The results of these preliminary bonding studies are shown in Table 5. These data show the quantitative nature of the evaluation of the wire bond results and an optimum combination of bond parameters. There are three types of bond configurations that can be achieved using the HPB-360 wire bonding machine. These are (1) a wire ball bond, (2) a wire lap bond, and (3) a ribbon lap bond. These bonds are pictured in Figures 17a, b, c. Each bonding surface was evaluated with each bond configuration. Table 5 should not be construed as a sole set of optimum parameters, indeed small variations in any one of the parameters might not produce any notable deviations in the results. Entirely different sets of parameters may also be found to produce the same results. These are shown merely to demonstrate the sets which were used to perform the environmental tests.

The wire pull test is performed by pulling the bonded wire in a direction 45 degrees off the normal to the bonding surface in a direction parallel to the bond wire and noting the maximum force attainable and the reason for breakage. All the bonds schedules which were selected as optimum sets demonstrated 100 percent center wire breakage at ~2.5 gms force for the circular wire and ~7.5 gms force for the strap, on assorted sample sizes, as opposed to other possible failure forms (e.g. bond lift, pad material lift, etc.). This provided the confidence necessary to proceed to the next step, that of subjecting the chip and package assembly to the environmental tests described above.

The bonding machine (Hughes model HPB-360) produces a thermal pulse (~475°C) at the point of contact between the bonding surface and bonding material with a selectable temperature pulse width while forcing the surface and material together. The heat is generated by driving a current pulse through a high resistance tungsten carbide capillary tool. The current pulse amplitude and width can be individually controlled to give the desired bonding results in conjunction with a preset amount of force between the bonded wire and bonded surface. The desired result is one wherein the degree of deformation of the bonding wire amounts to an increase in bond material width of 40 to 50 percent. As a rule, it is advisable to keep the heat pulse width as short as possible to avoid catastrophic differential thermal expansion and cracking of the garnet. The bonding temperature is kept moderately low to maintain long tool life and to avoid damage to the bond surface pads.

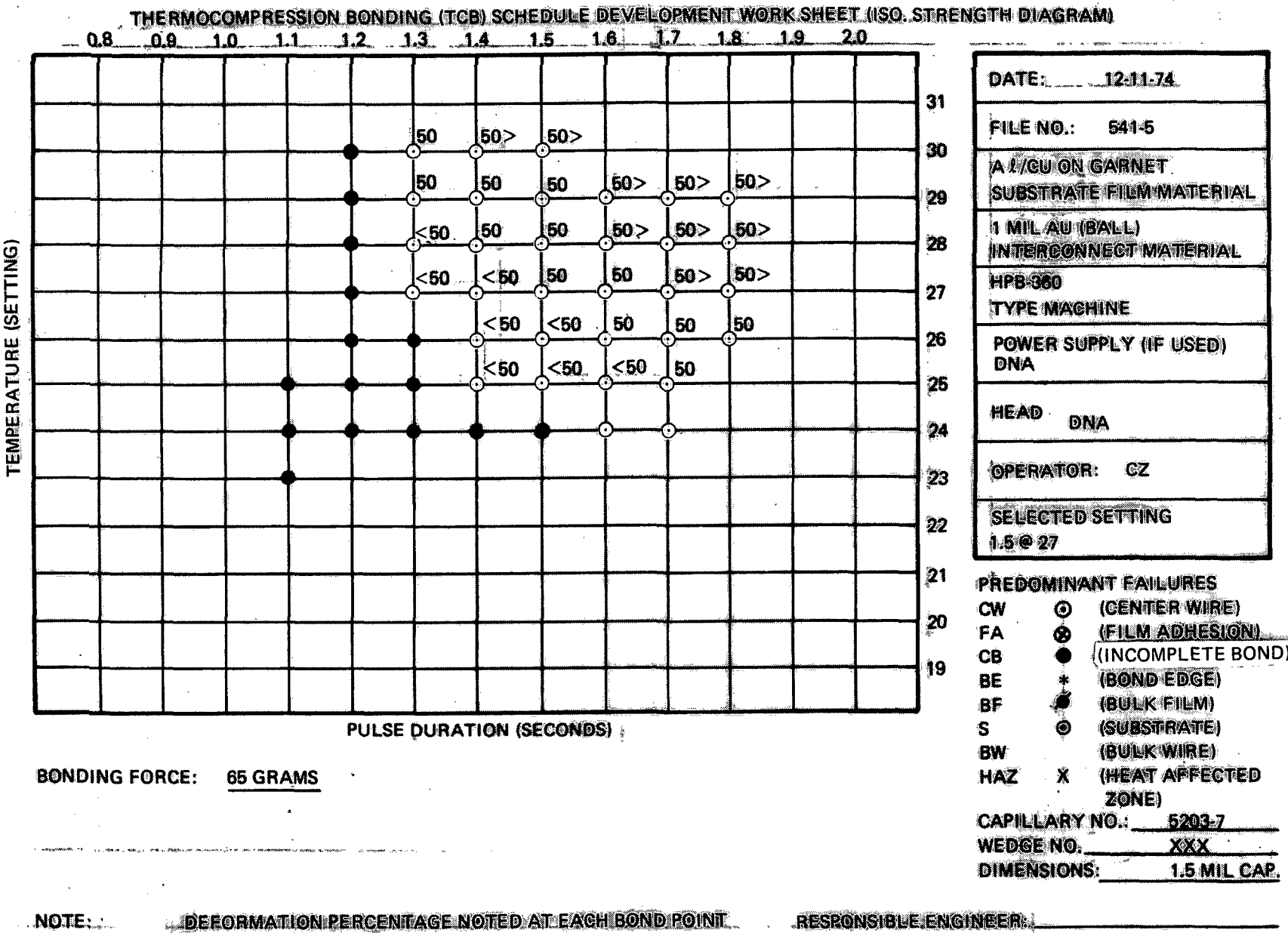

Figure 16. Typical Wire Bonding Parameter Schedule

TABLE 5. OPTIMIZED SETS OF WIRE BOND PARAMETERS*

Bond Material	Bond Type	Bonding Surface	Bond Force (gms)	Temperature Setting (nominal)	Temperature Pulsewidth (sec)
0.001 in. wire	Ball	Al/Cu on Garnet	65	27	1.5
0.001 in. wire	Ball	NiFe on Garnet	65	28	0.5
0.001 in. wire	Ball	Au/Cu on Polyimide	55	17	0.3
0.001 in. wire	Lap	Al/Cu on Garnet	55	25	1.2
0.001 in. wire	Lap	NiFe on Garnet	65	24	0.5
0.001 in. wire	Lap	Au/Cu on Polyimide	55	15	0.2
1 x 3 mil ribbon	Lap	Al/Cu on Garnet	55	27	1.2
1 x 3 mil ribbon	Lap	NiFe on Garnet	55	24	0.6
1 x 3 mil ribbon	Lap	Au/Cu on Polyimide	55	20	0.2

*(For a Hughes Thermal Pulse Bonder model HPB-360 to produce ~50 percent material deformation in dead soft gold.)

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After having chosen an optimum satisfactory bonding schedule set, the environmental tests were performed on ten bubble chips each mounted on polyimide-amide (Reference 23) die carrier test boards. Two of these chips were operating 100K bit devices, the other eight chips were not 100K chips but were fabricated using the same process technology. These eight chips were not functionally good shift registers but were selected because each chip had 30 bonding pad sites and hence allowed an increase of almost a factor of four in the bond integrity sample size for this evaluation compared to the 100K chip (eight bond pads/chip). Figure 18a and 18b shows a typical test package board and a 30 pad chip respectively. The test board package contained 30 connector contacts at the terminus of the board, (15 on top, 15 on bottom) and hence 15 vias through the board. The environmental testing then also tested the multilayer package capability of polyimide-amide printed circuit technology as well as the various bond to chip, bond to test package and die mount reliability of the chip assembly technology. The chip wiring diagram and a bonded chip is shown in Figure 19a and 19b.

Each test package board mounted chip was subjected to all the environmental tests sequentially. The 100K chips were operationally tested after each environmental test. The multi-pad chip assemblies were resistance measured at the test board terminus prior to the test series, subjected to all the environmental tests sequentially and remeasured again only after the whole environmental series was completed. Table 6 contains the test data for this set of eight devices. Both of the 100K bit devices operated with no distinguishable change in their 150 kHz operating margin characteristics all the way through the environmental stress. The data in Table 7 shows that changes in the average resistance values between pairs of board contacts are well within the tolerance of the measurement.

Note that there were 12 bond failures out of a total of 480 bonds made (240 total test board bonds and 240 total chip bonds). Of the 12 failed bonds, 7 were due to incomplete SiO_2 removal over the multipad chips. Two were due to excessive deformation of the bond wire at the chip bond site (see Figure 20a and 20b). Three failures occurred for post test high resistance values due to a very low contact area between the bond material and bond pad - probably due also to incomplete SiO_2 removal. None of the chip wire bonds on the good 100K bit chips failed and none of the failures occurred on the bond sites of the package test boards. The bond type, number and failures are shown in Table 8.

The conclusions which were reached as a result of this environmental test series are:

1. The wire bond and dice bonding techniques appear to be satisfactory - there are no serious failure modes in either the chip bond techniques or chip to package die attach techniques.

2. No major process modification will be necessary - although greater care must be paid to ascertaining that the SiO_2 etch over the Aℓ-Cu bonding pads is performed completely.

3. The die mounting technique (Ablestik 606-4 epoxy) is a good adhesive mounting for bubble devices.

4. The tests need not be re-run.

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TABLE 6. CONNECTOR RESISTANCE RESULTS FOR ENVIRONMENTAL TESTS

Board Connector/Terminal Identification	Bond and Material (1)	Bond Types (2) 1st Connector Die Pad	1st Connector Board Pad	2nd Connector Die Pad	2nd Connector Board Pad	Prestress Resistance Average Ω	Poststress Resistance Average Ω	Number of Bonds (3)	Total Bond Sets Failed	Type of Bond Failed W B	Type of Bond Failed W L	Type of Bond Failed R L	Category of Failure 1	Category of Failure 2	Category of Failure 3
1 - 2	W	B	L	L	B	58.8	59.0	32	Ø						
2 - 3	W	B	L	L	B	3.0	3.1	32	Ø						
4 - 5	W	B	L	L	B	3.0	3.0	28	1	✓			1		
6 - 30	W	B	L	B	L	57.0	57.7	32	Ø						
8 - 30	W	L	B	B	L	55.7	55.7	28	1						1
10 - 11	W	B	L	L	B	56.4	56.2	28	1						1
13 - 14	W	B	L	L	B	4.8	4.8	32	Ø						
14 - 15	W	B	L	L	B	2.8	3.0	28	1		✓			1	
16 - 17	R	L	L	L	L	4.8	4.8	24	2			✓	1		1
17 - 18	R	L	L	L	L	4.6	5.0	24	2			✓✓	2		
22 - 30	R - W	L	L	B	L	3.85	3.85	32	Ø						
24 - 30	R	L	L	L	L	54.4	55.0	32	Ø						
25 - 26	R	L	L	L	L	4.6	4.6	32	Ø						
27 - 28	R	L	L	L	L	4.3	4.6	24	2			✓✓	2		
29 - 30	R	L	L	L	L	57.0	58.0	24	2			✓✓	1	1	

NOTES:

1. "BOND MATERIAL" Legend: W = Wire (0.001" Dia. Au)
   R = Ribbon (0.001" x 0.003" Au)
2. "BOND TYPES" Legend: BALL-LAP = BL
   LAP-LAP = LL
3. Number of Bonds used to arrive at Pre and Poststress Average
4. Category of Failure: 1. Contamination on Chip Bonding Pad (SiO_2)
   2. Overdeformation of the Wire during bonding
   3. High Resistance (No visual cause)
5. All BOND FAILURES occurred on Chips.

TABLE 7. RESISTANCE STATISTICS OF CONNECTIONS SURVIVING THE ENVIRONMENTAL TEST SERIES

Initial Mean Resistance $\langle R_i \rangle$	25.09 Ω
Final Mean Resistance $\langle R_i \rangle$	25.27 Ω
Mean Fractional Change $\langle \Delta R_i / R_i \rangle$	0.0072
Fractional Mean Change $(\Delta R/R) = \frac{\Sigma \Delta R_i / \langle R_i \rangle}{432}$	0.0182
Standard Dev. of Fractional Mean Resistance Change	± 0.0283

TABLE 8. BOND SITE TYPES AND FAILURES

Bond Types	No. Bonds	No. Failed	Comments
Wire/ball on Al/Cu	44	1	SiO_2 contamination at bond site
Wire/ball on NiFe	28	1	Excessive deformation at bond site
Wire/ball on Au/Cu	56	0	
Wire/lap on Al/Cu	28	2	Indeterminate (probably SiO_2 contamination on bond pad)
Wire/lap on NiFe	28	0	
Wire/lap on Au/Cu	72	0	
Ribbon/lap on Al/Cu	56	7	(6) Contamination (SiO_2) on bond pad. (1) Excessive deformation
Ribbon/lap on NiFe	56	1	Indeterminate
Ribbon/lap on Au/Cu	112	0	

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5. MASK FABRICATION

5.1 Introduction

Over the years the procedure used to obtain masks for bubble devices has changed as a result of improvements in mask technology, device fabrication, and device performance requirements and design. Early masks were made by hand cutting rubylith at 400X or 800X and composing the pattern by hand if necessary. When device capacities reached 1K bit this approach became impractical. Computer aided design and computer controlled rubylith cutting techniques were then employed. The rubylith approach, however, still did not provide the precision necessary for bubble technology at this time because of the susceptibility of the large rubylith sheets to stretch or tear. A new approach was taken where the pattern is generated by direct photo plot onto a large emulsion film at ~150X. The machine used was a Gerber Model 2032 plotter which employed a number of fixed apertures on a rotable wheel. The aperture consisted of T, bars, chevrons, and small rectangles in various orientations. The proper apertures were chosen and stepped to compose the pattern by computer control. The repeatibility precision, that is the ability of the machine to return to the same location after a large excursion, was only ±0.1 mm which meant that the tolerance for a 1.6 μm gap (24 μm period) would be about ±25 percent. This is not acceptable for this size gap much less a 1 μm gap required for 16 μm period devices. In addition, it was very difficult to precisely center the apertures in the holder which also created tolerance problems in the final mask. Thus although the Gerber was suitable for circuit boards it was not satisfactory for bubble devices. This approach was abandoned as soon as a better machine was available. The present approach to pattern generation uses the David W. Mann Model 3000 pattern generator in which the bubble device is photo plotted at 10X directly on a flat emulsion/glass plate. This machine will be discussed further in Paragraph 5.3.

The mask fabrication procedure and the types of equipment employed will be discussed in the following paragraph. The basic steps followed in mask fabrication are summarized in Figure 21.

5.2 Computer Aided Design

After the engineering design has been completed, computer aided design (CAD) techniques are employed to massage the design into its final and precise form. A CALMA GDS (Graphic Design System) is used for the CAD. This system employs a Data General Nova II computer with a Caelus moving head disk. The design is generated using an interactive design station which consists of a keyboard computer input terminal and a TV monitor and light pen. Progress of the design can be reviewed on the TV monitor of the interactive station or by reproducing the design with a high speed pen plotter at a high magnification (~400X). In this manner the design can be reviewed and modified several times before the final design is reached.

To obtain a plotting tape for the Mann pattern generator after CAD is completed requires several steps as outlined in Figure 22. The output of the CALMA is a magnetic tape in which the design is coded in GDS machine language. A computer

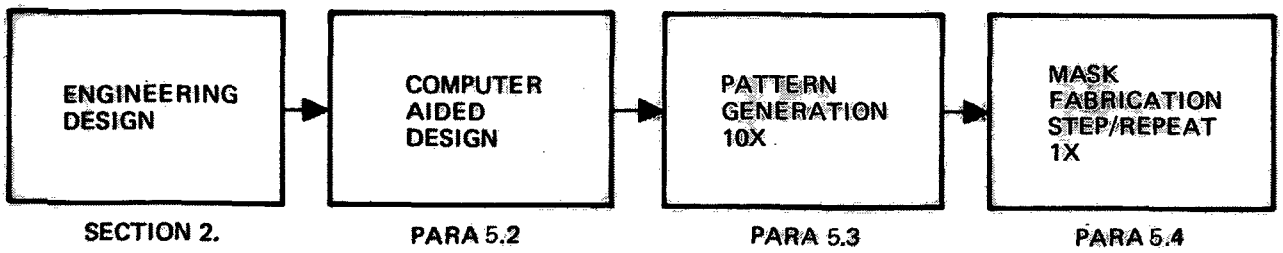

Figure 21. Steps in Mask Fabrication Procedure

translation is performed which converts the design to an LE (Line Encoding) language which is commonly used to describe geometric shapes (i.e., by general polygons denoted by line intercepts). The output at this point is a listing (and a computer card deck) which contains all the geometric shapes of the design. To plot these shapes on the Mann it is necessary to fracture these shapes into one or more simple rectangles. A computer program (LE-Mann translation) is available to do this. However, to conserve the number of flashes (which translate directly to mask cost) and to maintain a pattern precision many of the critical elements are fractured by hand which requires that a number of Rectangular Statements be inserted into the program. For a chevron element for example, four flashes are nominally used to approximate the desired shape. Computer fracturing of this element would result in about 16 to 20 flashes which would increase the plot time and cost considerably. At this point the design is translated from LE to LE-Mann language which the photo plotter can understand. However, one more step is required in which the flashes, which are now all coded as rectangular in various orientations, are again sorted by a program called G plot. Initially flashes were sorted as to X-coordinate position and angle. In this sorting a horizontal rectangle and a vertical rectangle whose centers were at the same X-coordinate had the same angle and would be plotted sequentially. This was the case for the H element in which the vertical, horizontal, and vertical rectangles of the H were plotted in that order. Since the distance between the vertical rectangles is only 16 microns, the aperture of the photo plotter had to change radically in a very short time. As the H-bar (or T-bar) is the major pattern of the device the plotting time was more than optimum (~8 hrs for a 100 K bit device). The plotting time was reduced (less than 6 hrs) by sorting to height and width as well as angle.

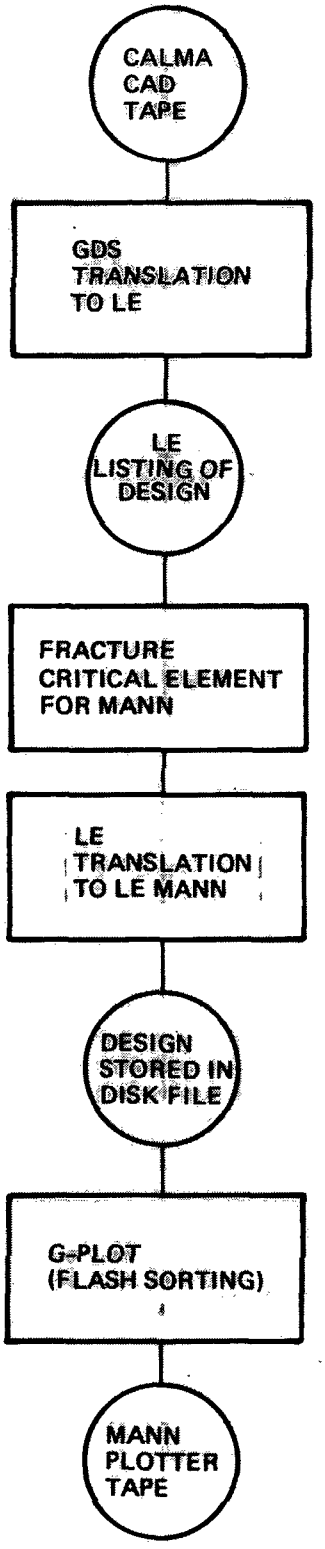

Figure 22. Sequence of Steps Leading from CAD to Completed Plot Tape

5.3 Pattern Generation

The Mann 3000 pattern generator is currently used for devices having resolution requirements down to 1 micron at 1X. This machine operates by a variable rectangular aperture which can be rotated to produce angles. The flash tube and aperture are fixed in position while the table holding the photo plate is moved. Its repeatibility precision is specified at ±0.25 m at the plot size (10X); however, in actuality about ±0.5 μm is observed. Some of this additional variation is due to the restriction that pattern placement by the plotter as well as in the CAD must fall on a grid which especially affects patterns that are at angles. The photo plotter is capable of about 80,000 flashes/hr, however, due to the complexity of the pattern and the flash sorting the average speed for plotting a propagation layer is about 41,000 flashes/hr. Thus for a T-bar type 100K bit serial device having approximately 250,000 flashes the plot time for the propagation layer is about 6 hr. Several areas of a 10X pattern generated original (PGO) of the propagation layer of M-1061 are shown in Figure 23. Each pattern element is made of one or more rectangular flashes which overlap to create the desired shape. The overlapping areas can cause some problem at this very high resolution because these areas are multiply exposed. These multiple exposures cause the edges of the pattern to grow which can cause a serious problem if it occurs in a gap region. This is an additional reason for hand fracturing the pattern element since it permits special care to be taken to avoid this problem. In the conductor where most of pattern is not critical hand fracturing is not required and multiple explosures present little problem.

5.4 Photomask Technology

The 10X magnification reticule produced either by photoreduction from higher magnification artwork or directly from a 10X PGO is photoreduced in the D. W. Mann model 3095 photo repeater. This machine is capable of achieving 1 μm photoresolution geometry at the 1X pattern size. Some other important capabilities of this photorepeater machine (although not necessarily unique or the best obtainable) are:

1. Position precision ±0.25μm
2. Position accuracy ±0.38μm
3. Orthogonality of movement ±1 sec of arc.

In order to achieve the degree of resolution and layer to layer registration alignment accuracy (±0.8μm) over a 2 in. square pattern array (8 x 8) needed for the 16μm period bubble device technology, proper environmental control is needed for this piece of equipment. Typically, it should be operated in a class 100 clean room environment with the temperature controlled to 20°C ±1°C and relative humidity controlled to the range of 30 to 40 percent.

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The light source for the photorepeater is a mercury-xenon lamp with a flash rate of 1/second for positive photoresist (Shipley AZ1350J). The 1X pattern is stepped across the face of the mask plate held in the moving fixture of the photorepeater optical column base. The mask plate blank is a "hard surface" material, e.g., iron oxide (Fe_2O_3) or nonreflectant chrome (oxidized chrome). The blank surface is uniformly coated with a thick film of positive photoresist (~1μm -AZ1350J). The exposed 1X pattern array mask is developed, the pattern etched and the photoresist removed.

Hard surface masks for this contract were made in both iron oxide and nonreflectant chrome surfaces. The photorepeater master mask was used as the working mask for the 16μm bubble technology. This was done because contact print copies of the photorepeat master suffer a reduction in resolution at these geometries just as do the patterns printed on the wafers. Going to an intermediate printing step (onto mask copies) introduces a second level of resolution loss which is not acceptable for the 16μm, 100K bit device compared to the cost savings of making work copies. This reduction is principally due to the inability to achieve uniform intimate contact over the interface between the contact planes of the mask plates. It has been our experience that a good hard surface master can be used on ~ 50 wafers before it has to be discarded.

The initial 100K bit device pattern array masks were fabricated on Fe_2O_3 mask plates. The resolution and uniformity of the resolution was very good. The first two yield runs used Fe_2O_3 masks; however, the quality of the vendor's Fe_2O_3 material seemed to degrade very substantially over a period of 6 months. The hardness of the Fe_2O_3 masks was intially very good, leading to a relatively long mask life. After the second yield run, new Fe_2O_3 masks shows signs of smearing and low abrasion resistance.

During this period, the non-reflecting "black" chrome mask blanks were evaluated and found to perform very satisfactorily. Consequently, a shift to this type of mask was made for the third yield run. More rigid mask inspection criteria were undertaken. It is important to realize that accurate visual inspection of a 100K bit pattern array (5 x 5 or larger) is an impractical approach. Each 100K propagation pattern has $\sim 4.0 \times 10^5$ gaps and pattern elements, with geometry resolution requirements between 2.25μm and 0.8μm. Without a computerized mask pattern inspection technique, the only reliable method of inspecting the pattern array is to check quasi-static propagation on a permalloy and SiO_2 coated wafer. Over a large number of wafers, an integrating map of device results will show those patterns in the mask array which were defective initially. Such an integrated mask array inventory based on the results from 16 wafers in the third yield run is shown in Figure 39. In this figure, the numbers of good devices are entered at each pattern site in the mask for all 16 wafers. The assumption is then, that those array points which never show a good device were defective patterns in the as-produced mask. Obviously for this particular mask, the number of good patterns resulted in a mask limited yield of 73 percent. This is a considerable deviation from the "assumed" mask yield of ≥90 percent as stated by the supplier. If we assume a mask defect sensitive area based on the yield model, this amounts to a defect density, including resolution variations as defects of 1.0 cm^{-2}. This is not insignificant when one considers that the total defect density introduced by the garnet film and circuit processing is about 8 cm^{-2}.

Clearly, the mask limited yield results alone imply that continued work at this pattern density with these required resolutions would benefit from a device design which is tolerant to both resolution variations and defects in the pattern.

5.5 Summary of the Photomask Fabrication Procedure

An outline of the mask fabrication is presented in flow diagram form in Figure 24. The major steps discussed in the preceding paragraphs are denoted by the rectangles. Several minor steps are required between these major steps and more importantly inspection steps where decisions are made to either proceed with the process or to go back to some earlier point and try again. The inspection steps get more difficult and involved as one gets farther into the mask fabrication process.

In the CAD step, inspection involves making sure that the data on the magnetic tape for the photo plotter is correct. Automatic pen plots of a major portion of the device are used to ensure that all the pattern elements are these and that they are approximately in the right position. Next partial photo plots of the unique portions of the pattern are made to check actual pattern dimensions and the composition of the individual elements. When an outside mask house has been used the final plotter tape is plotted in total before shipment to verify that the tape is good so that no plotter problem will be experienced by the vendor. A blowback (i.e., a 100X print of the PGO) is provided by the vendor after the pattern is plotted to ensure that no unforseen problem has occurred during pattern generation. Of course the quality of the vendor's process has been evaluated beforehand so that verbal confirmation of dimensional tolerances is all that is required at this point.

The next several inspection steps are performed by the mask vendor. Inspection is by visual means only and it is very time consuming and difficult. In general, only the overall mask quality can be determined because of the large number of pattern elements and gaps on the mask to be checked (4×10^5 elements and gaps per die). Before a mask is shipped the yield must be 80 to 90 percent by the vendor's inspection using a sampling of 25 percent of the mask die.

Upon receipt of the masks a brief visual inspection is made to ensure the general quality of the mask. Final inspection involves actually printing the mask on a number of wafers and electronically testing the devices using a wafer probe tester. If one or more die are found with margins of 10 Oe better, this is an indication that the 10X reticle used by the vendor is defect free so that no repeated defects appear in the mask array. If repeated defects are found, the vendor is requested to inspect his reticle and either reclean or replot and make additional masks.

The electronic test can also determine mask yield by processing a number of wafers so that the mask yield can be separated from the process yield. If a device corresponding to a given mask pattern passes the wafer level probe test it is proof that this mask pattern is good. On the other hand if another device on the same wafer fails the probe test it may be due to garnet or device processing defects unrelated to the mask pattern. If the second mask pattern is good it will eventually produce an acceptable device on another wafer if it is not damaged in the interim. Thus the die yield on the mask determined from wafer probe data is an increasing function of the number of wafers processed and asymptotically approaches the actual mask yield as shown in Figure 25. By this evaluation the mask yield must be near the 80 percent level or the masks are not accepted.

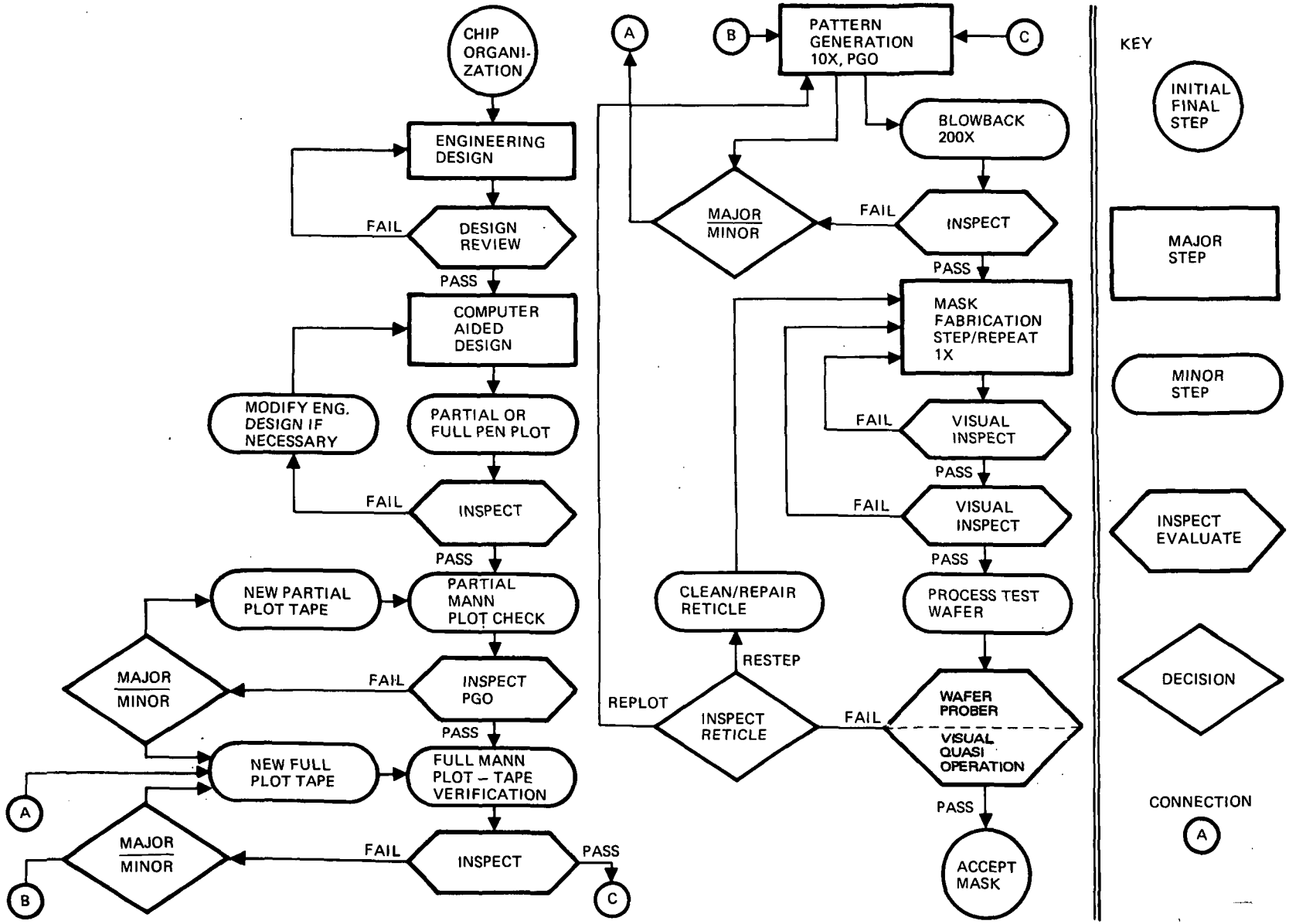


Figure 24. Outline Of Mask Design, Fabrication, Verification And Acceptance Procedures

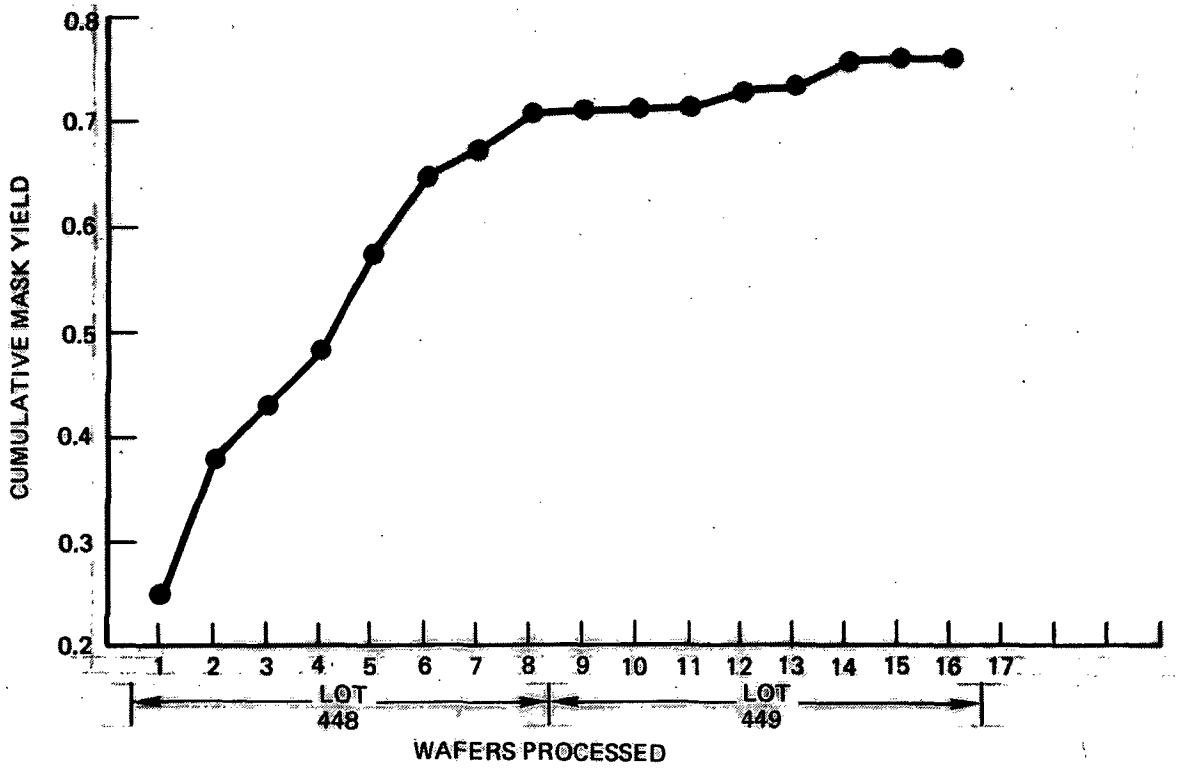


Figure 25. Cumulative Yield of a Pattern M-1067 Mask as a Function of Processed Wafer Sequence

6. BUBBLE DEVICE YIELD MODEL AND YIELD RESULTS

6.1 Yield Model

Several yield models have been constructed for application to the fabrication of bubble domain memory devices (Ref 24, 25). The model developed at Rockwell has been found through experience to be accurate in the prediction of fabrication yield of bubble devices. This section will discuss the yield model, present the yield results on three separate 100K bit bubble device fabrication runs, compare these results with the yield model and conclude with an analysis of the impact of serial loop fabrication yield versus several on-chip and off-chip redundant loop, fault tolerant chip designs.

6.1.1 Physical and Mathematical Formulation. - Generally speaking, defects in bubble devices are principally due to (1) magnetic defects in the epitaxial garnet film, (2) physical defects in the high density, high resolution permalloy pattern elements, (3) defects in the photolithography mask patterns and (4) defects created during post process handling, dicing, assembly, etc. The yield analayis presented here will deal with the first two defect sources. Yield losses associated with mask and handling defects can be treated by an experience multiplier in the overall process yield. For the typical high capacity bubble devices, i.e., 3 to 5 μm diameter bubbles. the nature of these defects, in a typical microelectronic device fabrication environment.

1. Small defect size
2. The probability of either defect type occurring at a specific site is low (i.e., a low defect density).
3. The number of affectable sites is high (i.e., a high density of defect sensitive sites).
4. Random distribution, without clustering tendencies.

Consider a device with area A_d located on a wafer with area A_w. Suppose that a single defect is placed randomly in the area A_w. The probability that it will not land on the device area in question is $(1-A_d/A_w)$. If a second defect is placed randomly on the wafer, it may fall on the particular chip of interest, or on another chip, or on the same chip as did the first defect. The probability that it fell on the particular chip of interest is, again, $(1-A_d/A_w)$. This idea can be extended to N total defects. The probability that the particular chip of interest survived these N defects is $(1 - A_d/A_w)^N$. Hence the yield is:

$$Y = (1 - A_d/A_w)^{nA_w} \tag{1}$$

where n is the average defect density per unit wafer area.

The binomial expansion of Eq. (1) looks like:

$$Y = 1 - N\left(\frac{A_d}{A_w}\right) + \frac{N(N-1)}{2!}\left(\frac{A_d}{A_w}\right)^2 - \frac{N(N-1)(N-2)}{3!}\left(\frac{A_d}{A_w}\right)^3 + \cdots$$

$$\cdots \frac{N!}{N!}\left(\frac{A_d}{A_w}\right)^n .$$

Notice that for large N ($\gtrsim$10) and small A_d/A_w ($\lesssim$10), this expression is similar to:

$$e^{-nx} = 1 - nx + \frac{n^2x^2}{2!} - \frac{n^3x^3}{3!} + \cdots$$

hence the probability of finding a bubble device with zero defects can be approximated by:

$$Y = \exp\left[-(nA_w)\frac{A_d}{A_w}\right] = \exp(-nA_d) \qquad (2)$$

where n is the defect density per unit area.

Equation (2) is simply the probability of finding a chip with defect sensitive area, A_d, in an ambient of defects with random distribution density n, which contains zero defects. This then is the Poisson equation:

$$P(x) = \left(\frac{\lambda^x e^{-\lambda}}{X!}\right)_{x=0} = e^{-\lambda} \qquad (3)$$

The general form of Eq. (3) states that the probability of finding a chip with x or less defects, whose (defect density) x (defect sensitive area) product is λ, is given by P(x). We will return to this general form later in this section when we discuss the yield run results.

Since the defect densities in the epitaxial garnet film and the fabricated circuit on top of the garnet have a zero correlation coefficient, the total fabrication yield for a serial shift register can be simply considered as the product of the P(0) functions for each contribution

$$Y_T = Y_A \cdot Y_G \cdot Y_C \qquad (4)$$

where $1-Y_G$ is the yield reduction due to garnet film defects.

$1-Y_C$ is the yield reduction due to circuit film defects.

$1-Y_A$ is the yield reduction due to non-Poisson defects (e.g., mask pattern defects, handling space damage, etc.).

now

$$Y_G(O) = \exp(-n_g A_g) \tag{5}$$

where n_g is the average density of defects in the garnet film and

A_g is the defect sensitive area of the garnet device or chip.

The factor A_g is more easily expressed as the total bit capacity (C_o) of the bubble chip divided by the bit density (D), which is simply the product of the number of defect sensitive sites and the area per site.

For a 16μm period bubble chip (D~3.9 x $10^5 cm^{-2}$) and

$$Y_G = \exp\left(-\frac{1}{2} \cdot \frac{n_g C_o}{D}\right) \tag{6}$$

(The factor of 1/2 used here assumes that the bubble only "sees" one half of the bit cell area, in other words, the actual defect sensitive area of the bit cell is one-half the cell area). Eq (6) has been plotted for several values of C_o in Figure 26.

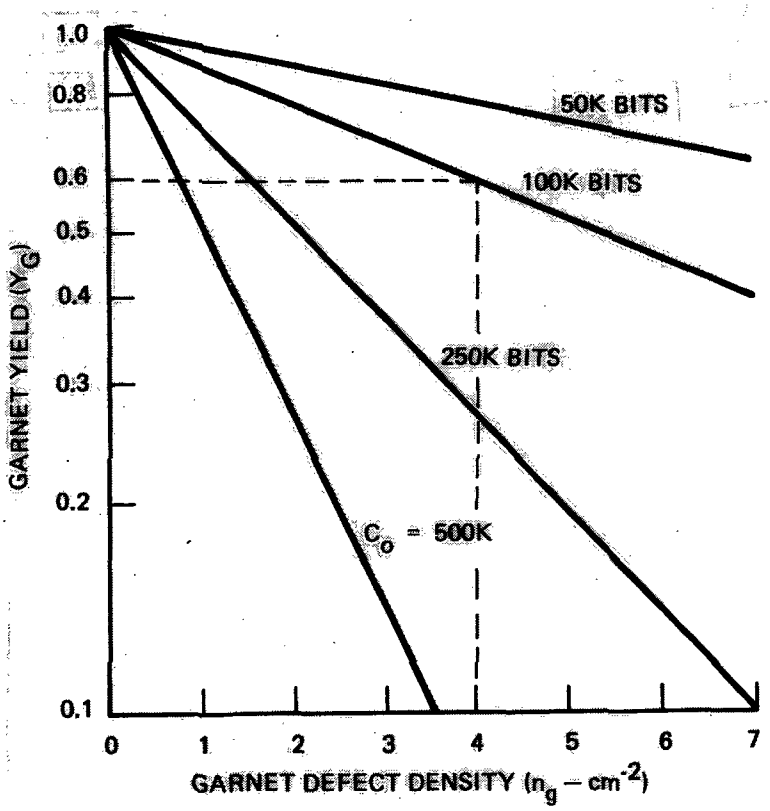


Figure 26. Garnet Yield vs. Garnet Defect Density for Several Values of Chip Capacity (K = 1024) (16 μm period)

The circuit fabrication yield factor has a form similar to Eq. (2) and is

$$Y_C = \exp(-n_c A_c) \tag{7}$$

where n_c is the circuit defect density

A_c is the defect sensitive circuit area

Since the permalloy film circuit elements represent a much larger defect sensitive area than that of the conductor pattern, we will assume that A_c is the active circuit area of the permalloy elements. This is tantamount to assuming a 100 percent yield on the conductor pattern lithography and etch step. This is not strictly true, however, a significant yield loss at this step would be cause for rework. The actual yield loss in completed devices, due to defects in the conductor pattern is sufficiently small to be essentially negligible. For a 100K bit, 16μm period serial loop chip, the active permalloy circuit area which is sensitive to defects must obviously be the same as the sensitive garnet area. Hence, $A_g = A_c = (C_o/2D) \simeq 0.13$ cm^2 for a 100K bit chip. The value of $n_g = 4$ is used throughout Section 6 for yield calculations on 16 μm period circuits. Our acceptance criteria for garnet films is $n_g \leq 4$ based on the results shown later in this section. Inserting this value in Eq. (6) gives $Y_G = 0.59$ for a 100K bit serial chip.

The defects in the circuit film are found to have a size dependent distribution for small defects encountered in the bubble circuits. Experiments in our laboratory have confirmed that the defects have a size probability distribution according to αx^{-3} where x is the mean diameter (cm) of the spot defect. The factor α is a product function of the cleanliness of the ambient to which the chips are exposed and the average exposure time.

6.1.2 Effect of Ambient Particle Count on Defect Density. - It will be assumed that the random circuit pattern defects which occur for the bubble devices arise entirely from photolithography related processes. Further it is assumed that the deposited circuit pattern films and the photomask patterns are entirely defect-free and that the photoresist is also free of foreign particle contaminants. The only remaining source of defects must be the environment and specifically airborne particles (dust).

If it is assumed that the airborne particle density is relatively low so that interaction between the particles is non-existent, these particles can be described as an ideal gas which obey the Maxwell-Boltzmann particle distribution laws. The number of particles with speeds between v and v + dv is determined only by their kinetic energies and is a function of

$$v^2 = v_x^2 + v_y^2 + v_z^2$$

The distribution function for the speed must be the product of three independent distribution functions for the velocity components v_x, v_y, v_z. Hence:

$$\frac{dN(v_x)}{N} = f(v_x^2)\, dv_x, \quad \frac{dN(v_y)}{N} = f(v_y^2)\, dv_y, \quad \frac{dN(v_z)}{N} = f(v_z^2)\, dv_z$$

and

$$\frac{dN(v)}{N} = F\,(v_x^2 + v_y^2 + v_z^2)\,dv_x\,dv_y\,dv_z = \overset{3}{\underset{1}{\pi}}\,f\,(v_i^2)\,dv_i$$

$\frac{dN(v)}{N}$ is the function of particles having velocities between v and v + dv and F is the three component distribution function which can be justified as the product of the three independent distribution functions.

The mathematical solution which satisfies each of the $f\,(v_i^2)$ differential equations is:

$$f\,(v_i^2) = Q \exp\,(-v_i^2/v_o^2)$$

Hence:

$$F\,(v_x^2 + v_y^2 + v_z^2) = Q^3 \exp\,[-(v_x^2 + v_y^2 + v_z^2)/v_o^2] = Q^3 \exp\,(-v^2/v_o^2)$$

The value of Q is obtained by noting that the integrals of $dN\,(v_i^2)$ must represent the total number of particles with velocities between $\pm\,\infty$ in the i^{th} direction.

$$\int_{\text{all space}} dN\,(v_x) = \int_{-\infty}^{\infty} NQ \exp\,(-v_x^2/v_o^2)\,dv_x = N$$

$$\therefore Q = (\pi v_o^2)^{-1/2}$$

hence:

$$F\,(v_x^2 + v_y^2 + v_z^2) = (\pi\,v_o^2)^{-3/2} \exp\,(-v^2/v_o^2)$$

This distribution function F gives the fraction of particles with speeds v $[= (v_x^2 + v_y^2 + v_s^2)^{1/2}]$ in a particular direction. There are other particles with velocities equal to the same value whose component velocities differ from the values selected and which are moving in different directions. The complete distribution function, $H\,(v^2)$, which represents all the particles with velocity v is:

$$\frac{dNv}{N} = H\,(v^2)\,dv = 4\pi\,v^2\,F\,(v_x^2 + v_y^2 + v_z^2)\,dv$$

and

$$H\,(v^2) = \frac{4\,V^2}{V_o^3\,\pi^{1/2}} \exp\,(-v^2/v_o^2)$$

Note that v_o is the most probable speed since at $\frac{dH\,(v^2)}{dv} = 0$, $v \equiv v_o\,(2Kt/m)^{1/2}$, (since $\overline{v^2} = 3kT/m$).

The rate at which these particles impinge upon a surface, in a closed volume may be derived by considering only those particles with velocity components perpendicular to the surface. If the density of particles/unit volume is N/V, the number of these which have specific velocity (v_x) to reach the impingement area in question is:

$$\frac{dN(v_x)}{N} = H(v_x^2)\, dv_x$$

Only a small fraction of these will be able to reach the impingement area surface in a time interval dt, i.e., those which are within the distance $v_x dt$. If A_w (wafer area) is the impingement area in question, the fraction of the total volume which contributes to the impingement rate is:

$$(v_x dt)\ A_w/V$$

hence the number of particles striking with velocity v_x is:

$$d^2N(v_x) = \frac{N}{V}\ A_w\ v_x\ H(v_x^2)\ dv_x\, dt$$

Since the particle velocities range from 0 to ∞, the number of particles impinging on the area A_w per unit time is given by:

$$\frac{dN}{A_w\, dt} = \frac{N}{V}\ \frac{v_o}{(4\pi)^{1/2}} = N_o \left(\frac{kT}{2\pi m}\right)^{1/2} \qquad (8)$$

where N_o is the airborne dust count (particles/volume)

k = is Boltzmann's Constant (1.38×10^{-16} ergs/°K)

T= temperature (Kelvin)

m = mass of the airborne contaminant

In order to get a meaningful answer, it will be necessary to compute an average value for the mass

$$m = \left(\frac{4\pi}{3}\right) \rho x^3$$

$$\langle m \rangle = \frac{\int m\alpha x^{-3} dx}{\int \alpha x^{-3} dx} = \frac{\int \left(\frac{4\pi}{3}\ \rho x^3\right) \cdot \left(\alpha x^{-3}\right) dx}{\int \alpha x^{-3} dx} = \frac{\frac{4\pi\rho}{3} \int dx}{\int_x^{-3} dx} \qquad (9)$$

The integration limits should be picked to be reasonable and representative of the real environment. There is a minimum circuit defect size below which the bubble will not be affected. The lower limits can be justified as ~0.1 d_o where d_o is the nominal bubble diameter (4 μm here) and the upper limit would certainly be not more than ~3 μm in a typical clean room environment. If we assume a nominal value for the particle mass density, ρ, to be ~2 gm/cm^3, the average airborne particulate

mass is ~8.2×10^{-12} gms. At room temperature, and assuming a unity sticking coefficient, the number of particles which contaminate the wafer surface per unit area and unit time is

$$\left(\frac{1}{A_w}\right) \frac{dN}{dt} = N_o \, (2.82 \times 10^{-2}) \, cm^{-2} \, sec^{-1} \tag{10}$$

Typical values of N for several values of N_o exposure time are shown in Table 9. Table 9 needs to be further qualified in that all environmental conditions, the major process steps are performed in Class 100 clean hoods. The wafer is exposed, periodically, to the ambient. Conditions of non-laminar air flow in the clean hoods will also result in a dilution of the filtered clean hood air with ambient air. The intent of this section is simply to show the effect on yield, as experienced in our laboratory environment, due to ambient dust count control.

Data taken in our laboratory (class 1000 ambient) of the defect size distribution as a function of the typical exposure time for a wafer has resulted in an experimental value of 2.8×10^{-8} for α. Hence, the circuit defect density is given by:

$$n_c = \int_{0.1\, d_o}^{\infty} \alpha x^{-3} \, dx \tag{11}$$

$\cong 4.1 \, cm^{-2}$ for a 4 μm bubble circuit in a class 1,000 ambient

When this value is compared with the values of N shown in Table 9 for a class 1000 environment, the integrated exposure time of the wafer to this ambient is ~70 min. This would be the equivalent exposure seen by the wafer from the time it is coated with photoresist until it is placed on the ion milling vacuum system. This is a very good estimate of the average exposure time. The circuit fabrication, with this value of n_c is given by:

$$Y_c = \exp\,[-(4.1)\,(0.13)] = 0.58$$

TABLE 9. VALUES OF THE DEFECT DENSITY FACTOR AND EXPOSURE TIME PRODUCT

Fabrication Environment (Particles/ft^3 diameters ≥ 0.5μm)	Defect Density, N (cm^{-2})	
	Integrated Exposure Time	
N_o	1 Hr	2 Hr
100,000	360	720
30,000	108	216
1,000	3.6	7.2
100	0.4	0.7

and the total yield is given by

$$Y_T = Y_A\, Y_G\, Y_C \qquad (12)$$
$$= Y_A\, (0.59)\, (0.58) \cong (0.34)\, Y_A$$

The term Y_A is a cumulative, non-Poisson yield term which simply reflects the care and precision with which the bubble wafer is treated during and after fabrication. This term is composed of wafer breakage, damage to dice due to handling (tweezers, etc), damage to dice as a result of the in-process testing, dicing, dice cleaning, bonding, etc. The factor Y_A should be controllable, with experience, to ≥ 0.7, giving an overall process yield of ≥ 25 percent for the 100K bit serial bubble chips. Note that the circuit fabrication yield in this yield model formulation does not depend upon circuit period. This is because the defect sensitive area (A_C) is proportional to the square of the bubble diameter whereas the defect density, n_c, is proportional the inverse of the square of the bubble diameter. The overall yield improvement due to period reduction occurs because of the improvement in garnet yield Y_G. This is shown in Figure 27 where the factor Y_G is plotted for a 100K bit chip, assuming a constant garnet defect density of 4 cm^{-2}, for a range of bubble device periods.

The 16 μm propagation period structure is the optimum yield point design, in the standard UV photolithography technology. This is because the propagation gaps in the 16 μm period T-bar pattern are designed to be ~0.9 μm. This gap width represents the nominal resolution limit attainable with standard photolithography due to diffraction effects.

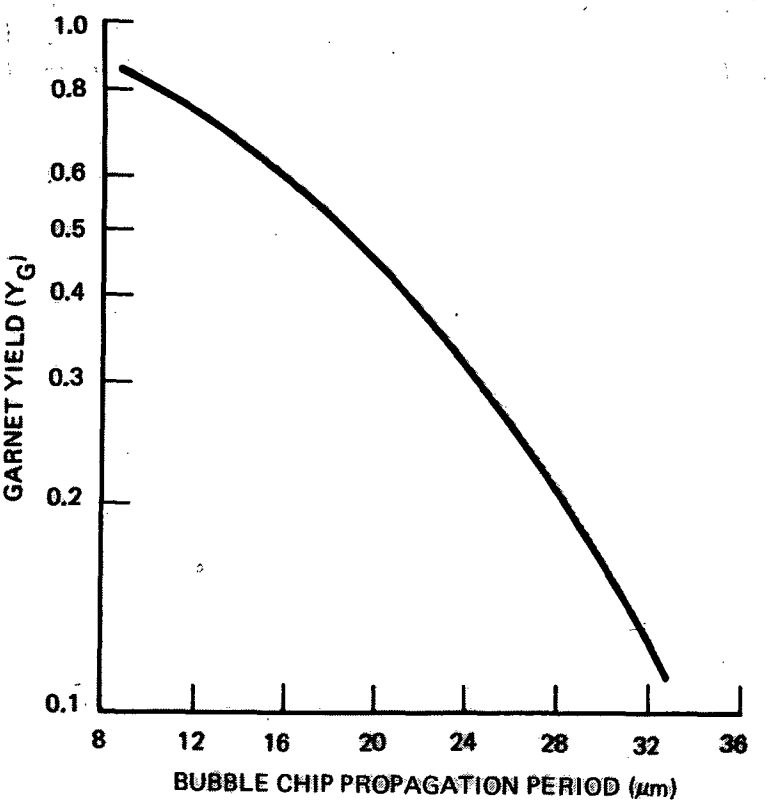


Figure 27. Garnet Yield vs. Propagation Period (C_o = 100K, ng = 4 cm^{-2})

6.2 Chip Fabrication Yield Runs

One of the principal goals of this contract was to demonstrate the producibility of the developed chip. Starting with a set of 50 unpolished substrates in a continuous process flow, we were to fabricate as many 100K bit memory elements as the process yield would permit. The losses in yield at each major process step were analyzed to determine the cause of the loss and the appropriate process modification were made in subsequent fabrication runs to minimize the incremental loss factors.

There were three distinct fabrication yield runs. Successive yield runs showed significant improvements in yield each time. The first two yield runs were made using 38 mm (1.5 in.) diameter wafers and the third yield run used 51 mm (2.0 in.) diameter wafers. The 38 mm diameter wafer can provide a maximum of 13 good dice as shown in Figure 28. The 51 mm diameter wafer will provide a maximum of 34 good dice shown in Figure 28. Photographs of 100K bit device arrays on 1.5 and 2.0 in. diameter wafers are shown in Figure 29. The usable diameter does not include the outer ~2.5 mm wide strip on the wafer edge. Figure 28 is drawn to scale with "effective" wafer diameters shown.

6.2.1 First Yield Run

6.2.1.1 Wafer Yield. - Fifty gadolinium gallium garnet (GGG) wafers (1.5 in. diameter) were sawn from a 1.5 in. center-less ground boule as purchased from a commercial supplier. These wafers were split into four groups for substrate polishing. Two wafers were broken at the polishing step. The liquid phase epitaxy (LPE) deposition ($Y_{2.62}Sm_{0.38}Ga_{1.15}Fe_{3.85}O_{12}$ nominal composition) was followed by a cursory film characterization for thickness, stripwidth and collapse field. One wafer was cracked during the epitaxial growth step but was characterized. The LPE garnet films were then implanted with Neon ($2\times10^{14}cm^{-2}$ at 80 keV) and subsequently thoroughly characterized. Table 10 shows the post implant results on the primary characteristics of the 48 films. In Table 10 the number of wafers shown (33) in the defect density column is principally a reflection of the polishing yield. Five of these films had defect densities between 5 and 10 cm^{-2}. The other 14 films had defect densities >10 cm^{-2}. These 14 films were not counted in the defect density statistics because wafers with obviously excessive defect densities are not mapped to completion and no numerical value exists for statistical purposes. The reasons for magnetic defects are: (1) unremoved saw damage, (2) substrate bulk defects, (3) residual surface contamination, and (4) defects induced by the LPE film growth process. The order of listing is also indicative of the order of importance. A complete description of the garnet wafer technology at the time of this fabrication run can be obtained in Ref 1.

6.2.1.2 Device Fabrication Yield. - The 33 wafers with defect densities less than 10 cm^{-2} constituted the first yield run wafer count at the start of device fabrication. One wafer was broken during the device fabrication processing. The device fabrication process requirements, especially film thicknesses, for the first yield run are shown in Table 11. The results on these deposition thicknesses for the yield run are shown in Figures 30 through 33. All the Al/Cu film depositions hit the specified thickness within tolerance. This film is electron beam evaporated and the depositing film thickness is monitored with a quartz crystal oscillator.. The control of the sputtered SiO_2 barrier layer thickness presented the most difficulty. Day-to-day fluctuations in the resistivity of the coolant fluid to the sputter cathode resulted in the large variations in deposition thickness of this film. The same problem is also

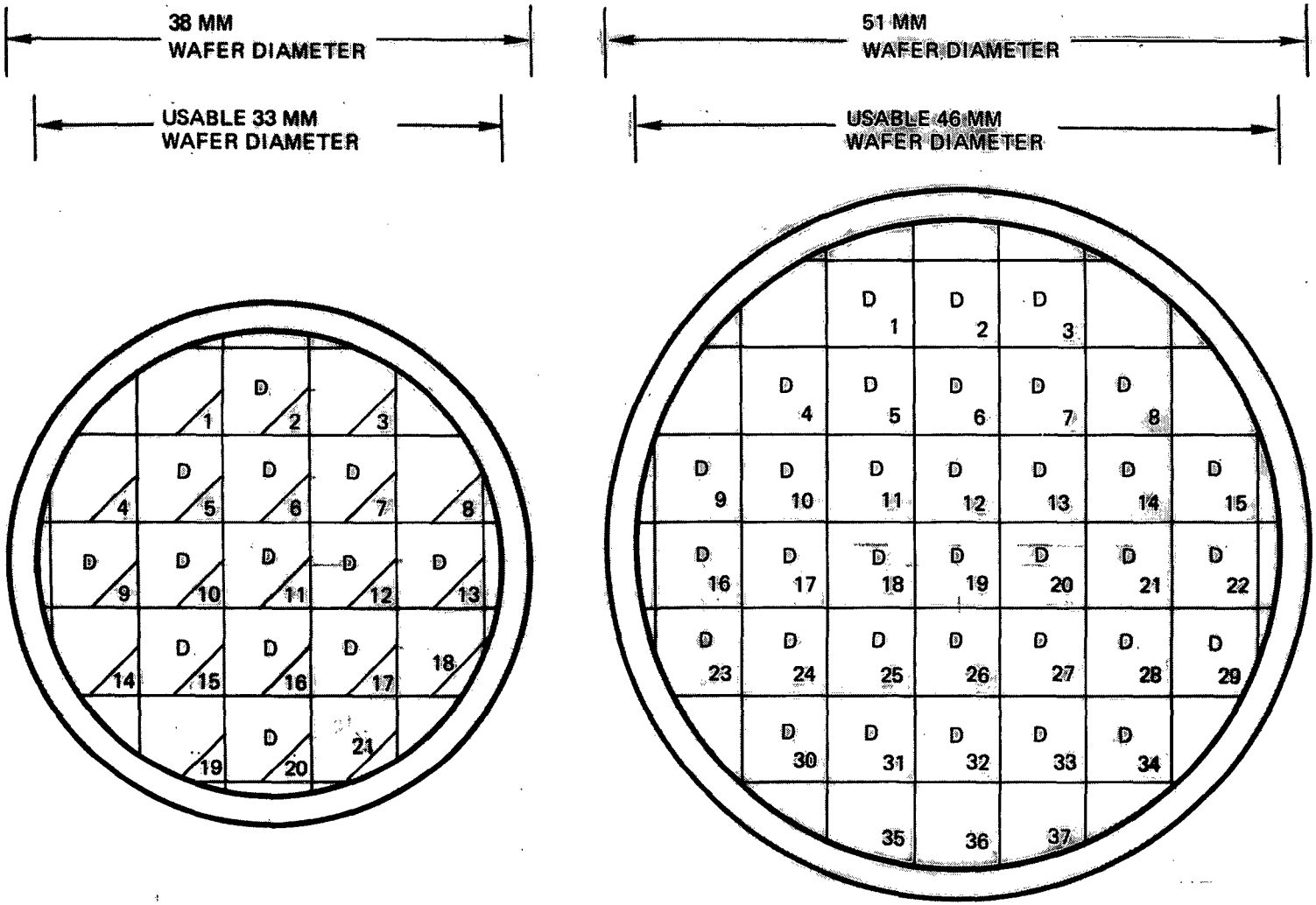


Figure 28. Arrays of Potentially Good Dice on 38 mm and 51 mm Dice Wafers

(a) M-1050 PATTERNS ON 1.5" DIA WAFER

(b) M-1067 PATTERNS ON 2.0" DIA WAFER

Figure 29. 100K Bit Devices on Garnet Wafers

TABLE 10. POST-IMPLANT CHARACTERISTICS OF THE WAFERS FOR THE FIRST YIELD RUN

	Film Thickness H (μm)	Strip Width W (μm)	Collapse Field H_{Coll} (Oe)	Saturation Magnetization $4\pi M_s$ (Gauss)	Defect Density (Ave-cm^{-2})
Maximum	4.05	4.41	125.60	248.00	10.00
Minimum	3.19	4.00	98.40	213.00	0.0
Mean	3.49	4.08	105.60	231.00	3.20
Std. Dev. (±σ)	0.16	0.08	4.94	6.11	2.58
No. of Films	48	48	48	48	33

TABLE 11. DEVICE PROCESS REQUIREMENTS FOR FIRST YIELD RUN

Parameter	Target Value
SiO_2 Barrier Layer (Sputtered)	1000 ±200Å
Al/Cu Conductor Layer (≤6 μ Ω cm) (e-beam)	5000 ±250Å
SiO_2 Spacer Layer (Sputtered)	7000 ±350Å
NiFe (H_c < 1.5 Oe, ρ_r > 2.5%)	4000 ±350Å
Propagation Pattern Line Width	3.0 ± 0.2 μ m
Propagation Pattern Gap Width	1.2 ± 0.1 μ m

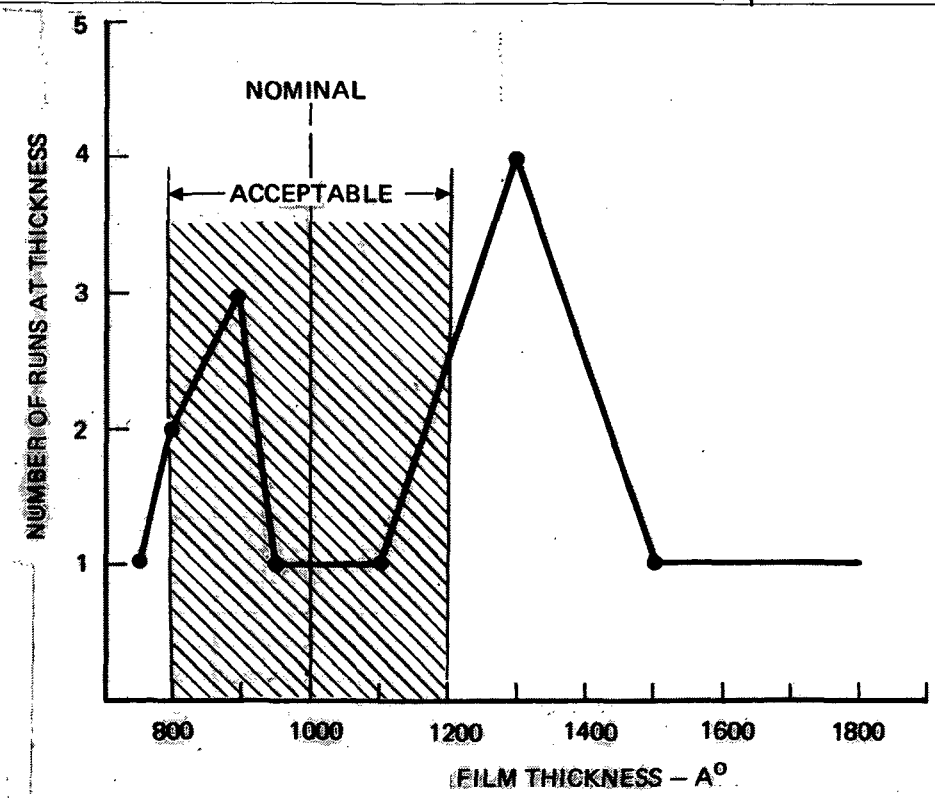


Figure 30. SiO_2 Barrier Film Thickness Lot-to-Lot Variation

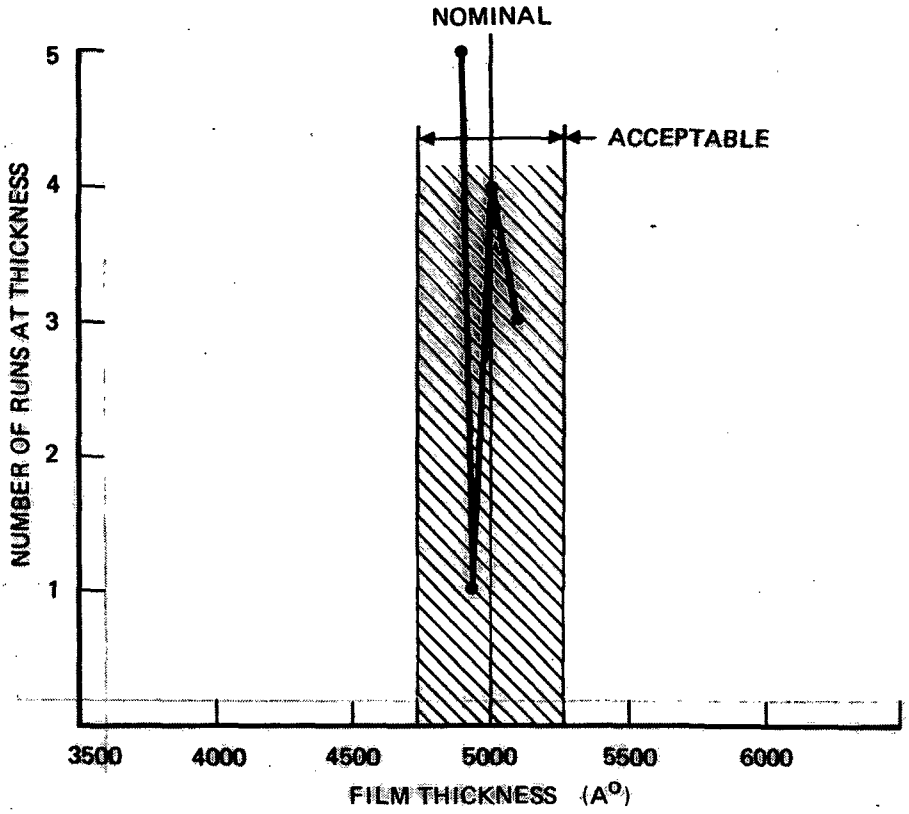


Figure 31. Al-4 percent Cu Conductor Film Thickness Lot-to-Lot Variation

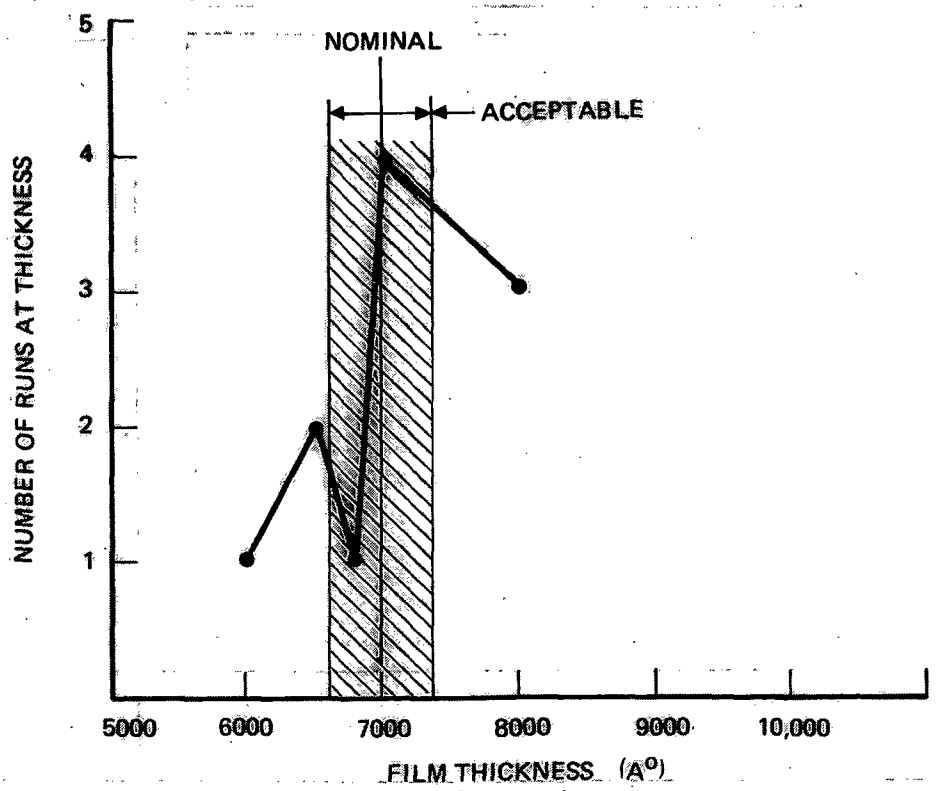
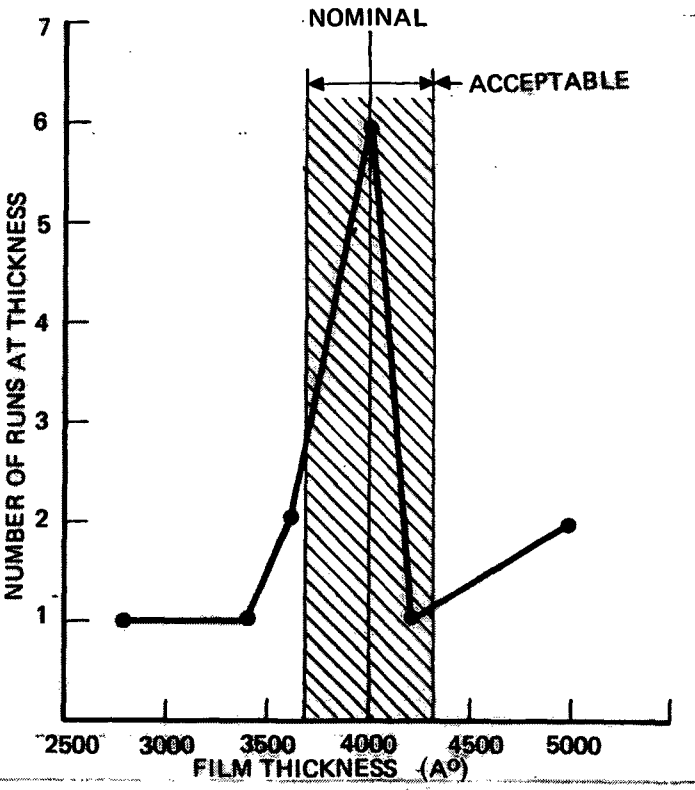


Figure 32. SiO_2 Spacer Film Thickness Lot-to-Lot Variation



PROPERTY	LOW	AVERAGE	HIGH
COERCIVITY (Oe)	0.35	0.42	0.50
MAGNETORESISTIVITY (%)	2.77	3.00	3.48

Figure 33. Permalloy (NiFe) Film Thickness Lot-to-Lot Variation

apparent in the sputtered SiO_2 spacer and NiFe films, albeit to a lesser extent. (The two thinnest permalloy films were stripped and redeposited, hence there are two more permalloy depositions than SiO_2 spacer depositions shown in these figures.)

The most serious fabrication problem in the first yield run was the large variation in the permalloy propagation pattern gap widths from wafer to wafer. Figure 34 shows a histogram of measured ratios of the linewidth to gapwidth as determined from photographs of identical pattern points on 84 dice from all 33 wafers. Using any criteria of judgement or speculation as to accuracy and precision of the measurement, it is seen that this parameter was not under control. The 100K bit pattern has a designed ratio range of 2.9:1 to 2.2:1 with a target ratio of 2.5:1.

The large variation in gapwidth was principally due to the pattern definition technique. For this yield run, the photolithography patterned wafers were ion milled. However the ion milling process was stopped with ~ 200Å of NiFe remaining on the wafer surface. The wafer was then polish etched in 30:9:1-H_2SO_4:H_2O:H_2O_2 to remove the remaining thin permalloy film. The uncontrollability of the etch rate resulted in irregular and excessive amounts of permalloy being removed from the pattern sidewall and hence large variations in the gap width. This chemical polish etch was abandoned in subsequent process runs and the large gapwidth variation problem has not recurred. Smaller (±0.2) variations in the ratio, with ratios which average close to the design value, are typically the results of slight deviations from intimate photolithography contact caused by non flatness of the wafer or mask or both and by minor variations in the photoresist process such as developing etc. These can be minimized but not avoided entirely.

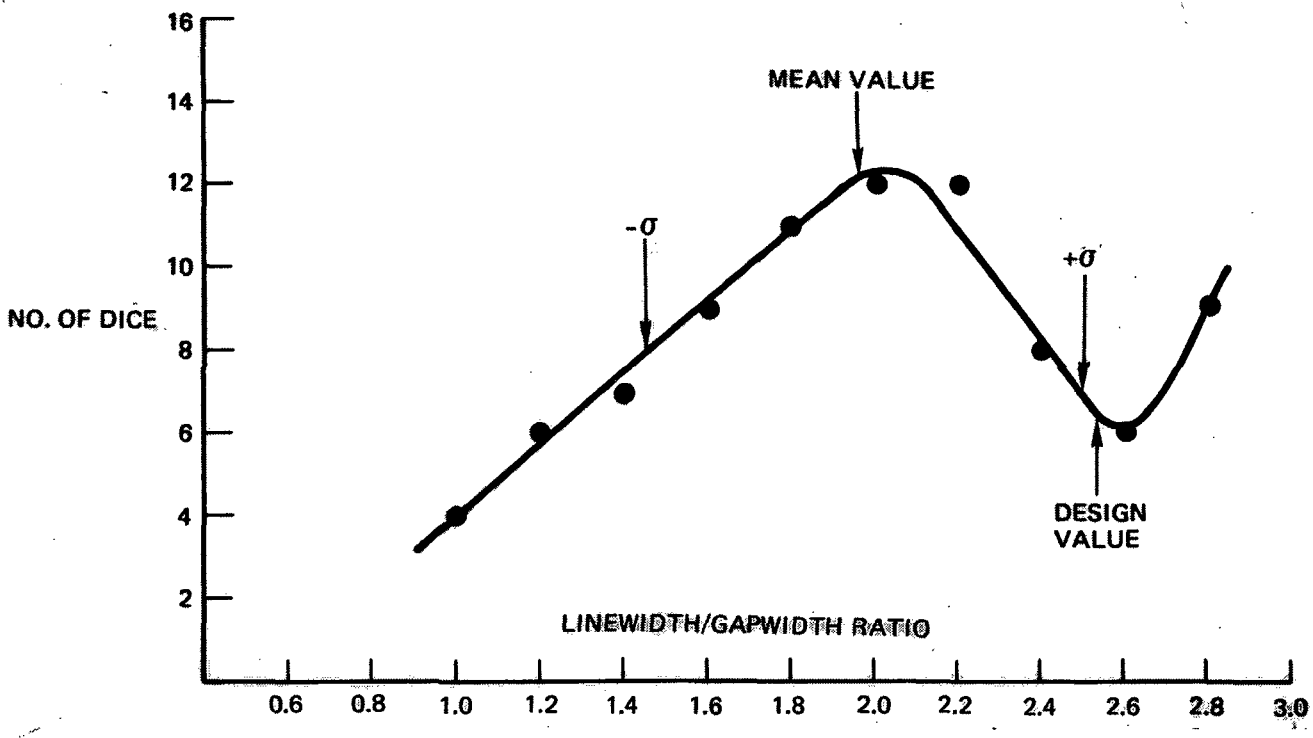


Figure 34. Histogram of Linewidth to Gapwidth Ratios for 84 100K Bit Devices

The wafers were visually inspected and mapped using high magnification microscopy at this point. Each die was examined for defects and a record made of the dice which contained no visual defects. The yield determined by this inspection was 130 good dice out of a possible 352. This placed the yield due to process induced defects at $\leq$ 37 percent. (The number of total possible good dice is the product of 32 wafers and an average number of good patterns/mask over the yield run of 11.)

6.2.1.3 In-Process Testing Yield. - The fabricated wafers (complete except for the opening of the conductor contacts) were tested quasistatically at 25 kHz, gated mode, visual observation for the first yield run. This wafer level test was considered an in-process test since the wafer was reworkable at this point - i.e., it was not diced. The test consisted of gating, in an open coil structure, a fixed bubble array pattern from column to column through the entire register and visually ascertaining the fidelity of the propagation in one complete register cycle. Quantitatively, this amounted to determining that the chip had a minimum margin of ~2 Oe.

The quasistatic (25 kHz) in-process test resulted in 40 operational dice. This apparent drastic reduction in the number of good dice from the visual inspection can be attributed to (1) the non-visually detectable magnetic defects in the garnet film (Y_g ~0.6), (2) the confidence level of visual observation of defects (estimated to be 0.8 to 0.9), and (3) handling damage (perhaps up to ~20 percent of the visually determined defect free dice were damaged by handling subsequent to the first visual yield inspection). However, for the first yield run, the in-process test technique also served as a strong feedback factor for the fabrication effort because visual observation of the defects could be used to assist in establishing in-process pattern

inspection goals. Visual inspection was performed again after the wafer level test and each of the yield run dice was inventoried for defects according to defect type and number of times the defect type occurred on the die. Again, the visual inspection yield was significantly higher than the operational test yield (see Table 13). This is a manifestation of the fact that no visual defects could be found in some of the dice which failed the wafer level operational test. Obviously, the operational test reveals defects which even the microscopic magnification does not reveal as well as those defects which will be missed during visual inspection no matter how carefully the inspector performs the task. The results of this defect inventory are shown in Table 12.

6.2.1.4 Post Fabrication Yield. - After the in-process wafer testing step, the wafers were diced, the good dice were mounted on test boards and the individual die characterization was performed. The dicing for the first yield run was performed on a continuous loop wire saw. Prior to the dicing operation, the wafer was treated as described in Para 3.5. After dicing, the dice were cleaned and examined. Prior to each die being mounted on the test board, it was again cleaned, as described in Para 3.5. The die was bonded to the test board with a thermocuring epoxy while being held in place with tweezers. The wire bonding of the die was performed with a thermal pulse bonder (Hughes HPB-360).

The excessive amount of handling which occurred after the in-process wafer test and the relatively harsh dicing, cleaning and mounting procedure resulted in a large number of good dice being damaged. This can be seen by the fact that only 19 good dice were obtained from the individual die characterization test.

The individual die test was performed at 150 kHz. Some of the good dice which were not damaged between wafer test and die test would not operate at 150 kHz, however the dominant reason for the failure of previously determined good dice was due to defects induced since the 25 kHz gated testing.

6.2.1.5 First Yield Run Summary. - Table 13 summarizes the first yield run results in terms of the major definable process steps. As a result of the information gained during the first process run, and in accordance with the topics discussed under the various headings, a number of process modifications were recommended. The following outline describes the major modifications, and in most instances, the reasons are obvious and self-explanatory in light of the aforementioned first yield run results.

Process Modifications

I. Garnet Wafer Technology

A. Improve surface polish to reduce defect density

1. Install a new polishing machine

2. Lap and polish wafer backside first
   Lap and polish wafer epitaxial side last.

3. Use chemical etch in addition to mechanical polish

TABLE 12. DEFECT DISTRIBUTION AND FREQUENCY OF OCCURRENCE

Defect Type	Percentage of Dice with n Defects							
	0	1	2	3	4	5	6	≥7
Garnet	64.8	22.4	7.5	4.4	0.9	-	-	-
SiO_2	86.0	11.1	2.0	0.6	0.3	-	-	-
Conductor	83.8	13.9	1.7	0.6	-	-	-	-
Permalloy	88.9	9.4	1.4	0.3	-	-	-	-
Propagation Photolithography	49.1	28.9	13.9	4.9	1.2	1.2	0.3	0.5
Ion Milling Cleanup	80.5	16.9	2.0	0.6	-	-	-	-
Handling	95.7	4.3	-	-	-	-	-	-

TABLE 13. FIRST YIELD RUN SUMMARY

Process (wafer)	Cumulative Yield	Comments
Polish	0.96	Two wafers broken
LPE Film Growth	0.94	One wafer cracked
Ion Implantation	0.94	
Characterization	0.66	14 films rejected for defect density $>10/cm^2$
Process (device)	**Cumulative Yield**	**Comments**
Wafer fabrication (visual inspection)	0.37	Yield due to process induced defects (one wafer broken)
In-process testing	0.114	Includes garnet yield factor (40 "good" dice)
Visual Inspection	0.157	After in-process testing
Operational test (150kHz)	0.054	19 operational dice

B. Garnet LPE Film Process

1. Replace the flux etch polish with an acid etch polish

2. Increase the post deposition spin rate

II. Photomasks - Generate the artwork at 10X on a Mann 3000 photoplotter - discontinue the use of a Gerber photoplot at 150X. This will achieve higher pattern geometry accuracy - fewer pattern errors.

III. Device Processing

A. Film Deposition

1. Install a closed loop coolant system on the sputter cathodes using a stable, high resistivity fluid.

2. Install a sputter deposition thickness and rate monitor to improve the control of the sputter deposition process

B. Closer photoresist pattern in-process control is needed. Strip and rework the photoresist pattern if visual inspection reveals excessive defect density or inadequate resolution.

C. Ion mill the permalloy layer all the way through, delete the polish etch step

IV. Device Testing and Characterization

A. Eliminate the 25 kHz gated visual testing procedure

B. Perform individual in-process dice testing on a wafer prober

C. Develop more realistic acceptance criteria for device parameters.

V. Post Fabrication Process Damage Control

A. Replace wire sawing with laser scribe and break

B. Develop an acceptable, low cost, protective coating technique to reduce the incidence of dice pattern damage due to post fabrication handling.

Examination of the dice which were acceptable from this first yield run demonstrated several types of permalloy defects which apparently are acceptable under the operating test conditions. The most prominent type was excess permalloy spots located either on the pattern element sides or in the clear field of the pattern. The one defect type which was not found in the good dice was excess permalloy in the gaps indicating that this is not a tolerable defect. One good die had a relatively large LPE process flux ring in the garnet layer and yet continued to operate, however none of the good dice had crystalline type garnet defects, indicating that these are critical defects.

As can be seen in Table 12., the defect types most prevalent in the dice patterns were due to photolithography defects introduced primarily as a result of the contact alignment and expose step, and the garnet epitaxial defects. The two most prominent lithography defects were caused by patterned resist elements lifting and defects due to foreign matter particles. The resist lifting is simply due to poor adhesion and the foreign particles demonstrate the need for tighter control on the ambient particle count, the amount of time that the photoresist coated wafer is exposed to the ambient, the cleanliness of the photomasks and the cleaning maintenance on the aligner equipment. Improved cleaning techniques and more rigid inspection requirements will reduce the garnet film defect density.

An examination of the linewidth to gapwidth ratio showed that operational devices had ratios which varied from 1.6 to 2.8. An attempt to correlate the operating margin, energy well depth, and the linewidth to gapwidth ratio showed a general trend for the higher ratio to have a lower operating margin. There is, however, considerable scatter in these data, due to a large variety of contingencies, e.g., too large a l.w./g.w. design ratio, too large a linewidth design (3μm), device process control (SiO_2 thickness and NiFe thickness variations from lot to lot) non-optimized device function designs (corners, merges, etc.). Various attempts to account for some or all of these variables did not improve the data scatter however.

The magnitude and range of the bias margins of the operational dice from the first yield run at a drive field of 80 Oe are shown in Figure 35. A typical bias field vs drive field margin for these devices is shown in Figure 45. These data simply show the nonconsecutive bit propagating margins at room temperature (25°C). The high drive field required is probably due to a combination of circumstances: (1) the wide linewidth (3 μm), (2) the large gap-width (typically 1.3 to 1.9 μm), and (3) corner design in this pattern, to name the most important. The number of "good" operating devices from this yield run exceeded expectations but the more important factor was the learning, through experience, to be applied to the development of the bubble fabrication technology.

6.2.2 Second Yield Run

6.2.2.1 Wafer Processing. - In the light of the results on the first yield run as well as experience derived from work on other contractual efforts and company supported programs, the garnet substrate and garnet epitaxial film deposition techniques were reviewed. Out of this review, garnet wafer process modifications were introduced with a goal of increasing the garnet film yield and reducing the material cost. The garnet wafer portion of the second yield run was started using the modified processes and different equipment described as follows:

1. GGG boule surface polishing - the 38 mm (1.5 in.) diameter (centerless ground) boule was tumble polished in a one liter nylon lined container using 6mm diameter glass beads with first a deionized water slurry of 12 μm Al_2O_3 as the abrasive and next with a slurry of 0.3μm Al_2O_3 (Linde A). The boule was rolled on a two roller mill for 24 hr. in each abrasive polish mixture. The resulting boule had a highly polished surface which enhanced the boule material inspection and also removed the boule surface damage due to centerless grinding.

2. Wafer slicing - an I.D. diamond saw was used to slice the boule into 0.76 mm (0.030 in.) thick wafers. The blade was 0.3 mm (0.012 in.) thick and the slicing kerf loss was ~0.38 mm (0.015 in.). The blade speed was 2800 RPM resulting in a cutting edge velocity of ~0.9 km/min. The boule feed rate was ~7.6 mm/min (0.3 in./min.). The wafers were inspected and sorted for cut surface finish, slice uniformity, surface flatness and warpage. From a sampling of the cut wafers, none had more than a 25μm thickness variation and the cut surface quality was very good.

3. Wafer Lapping - The wafers were mounted with wax onto a 27 cm (10.5 in.) diameter plate and lapped on a 24 in. Lapmaster machine using a slurry containing 9μm alumina abrasive, Do-all cutting fluid and water. Sufficient material is removed during this operation to eliminate the slicing saw induced damage, with minimal residual surface damage remaining due to the lapping slurry. This step also maintains the coplanarity of the two wafer surfaces.

4. Substrate Polishing - The surface polishing process was performed on a 26 in. Strasbaugh Polishmaster machine (Model 6BL). This is a four spindle machine with motor driven spindle rotation and improved pressure and temperature control compared to the equipment used previously. The

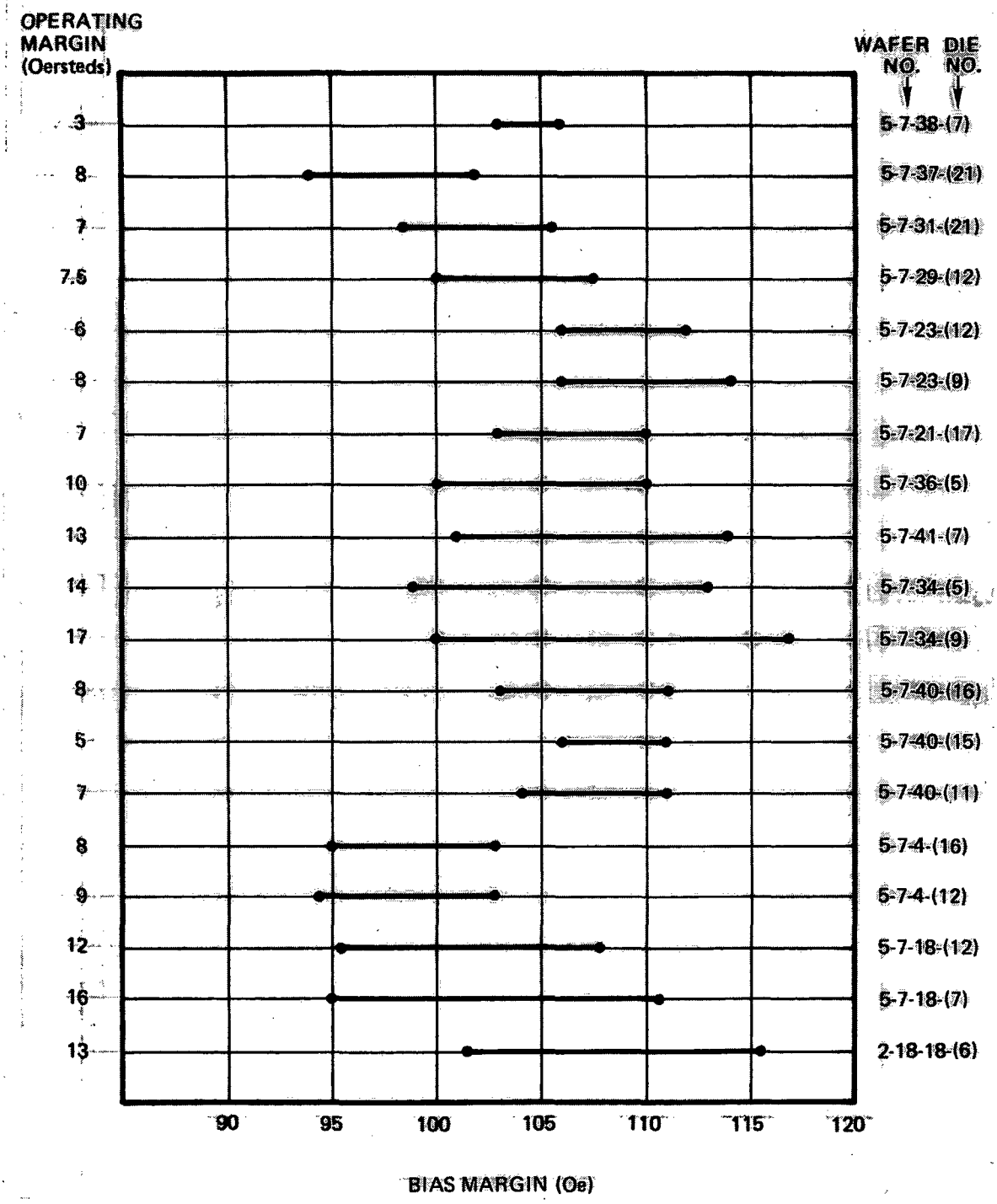


Figure 35. Bias Margins for First Yield Run Devices
(150 kHz, Alternate Bit, 25°C)

polishing abrasive was still the Syton/H_2O mixture. This polishing step removes ~25μm from the backside of the wafer. The wafers were then turned over and the front (epi) side was polished to remove ~50μm of material. The new equipment improved the polishing removal rates with improved mechanical reliability resulting in a more reproducible process.

Fifty GGG wafers were produced in-house from a commercially purchased centerless ground boule. The wafers were polish processed as described above. One wafer was broken during the demounting step after wafer lapping. Prior to the LPE garnet film deposition, each wafer was etched in a hot (200C) solution of H_3PO_4: H_2SO_4 (1:1) for two minutes. The etch removed ≈1μm of GGG from the polished epi surface. This process step replaced the previously used flux polish resulting in fewer flux rings (mesas) and improved wafer flatness. This chemical etch step is more amenable to batch process techniques resulting in a lower process cost.

The epitaxial garnet film composition for the second yield run was the same as the first yield run. The target properties for the second yield run are shown in Table 14.

TABLE 14. TARGET GARNET FILM PROPERTIES (SECOND YIELD RUN)

Property	Target	Acceptable Range
Film Thickness	3.5μm	±5%
Stripwidth	4.0μm	±5%
Collapse Field	110 Oe	±5%
Defect Density	≤4 cm^{-2}	-

The actual parameter values of the wafers grown with epitaxial garnet are shown in Table 15.

TABLE 15. GARNET FILM PROPERTIES AFTER ION IMPLANT (44 WAFERS)

Parameter	Mean Value	Standard Deviation (± σ)
Film Thickness	3.44	0.135 μm
Stripwidth	4.10	0.248 μm
Collapse Field	109.00	10.23 Oe
Defect Density (40 wafers)	4.00	2.29 cm^{-2}

The defect density values shown in Table 15 apply only to 40 wafers because those wafers with defect densities >10 cm^{-2} are simply characterized as high. The defect density distribution for all 44 wafers is shown in Figure 36. Notice that the wafer defect densities show a log normal distribution.

There were 49 polished substrates submitted for LPE film growth. One substrate broke during the pre-deposit hot acid etch probably due to thermal shock or the result of an undetected crack on the wafer edge. Nine LPE films had been grown when a leak was detected in the crucible. A new crucible and melt was initiated and the LPE growth series restarted. Of the 49 wafers submitted for film growth, four were lost in the LPE melt. It was found that the quicker response alternating rotation motor and higher post deposition spin rates were responsible for this problem. This problem was solved by replacing the pure platinum wafer holding fixture with a Pt/5 percent Au alloy to improve the fixture holding strength. This change cured the problem of wafer loss in the melt. Two wafers cracked during cooldown after LPE deposition. These wafers, though not delivered for device process were, nonetheless, characterized and their data included in Table 15. About midway through the LPE series, on an intermittent basis, high defect densities were encountered. The cause was traced to platinum contamination.

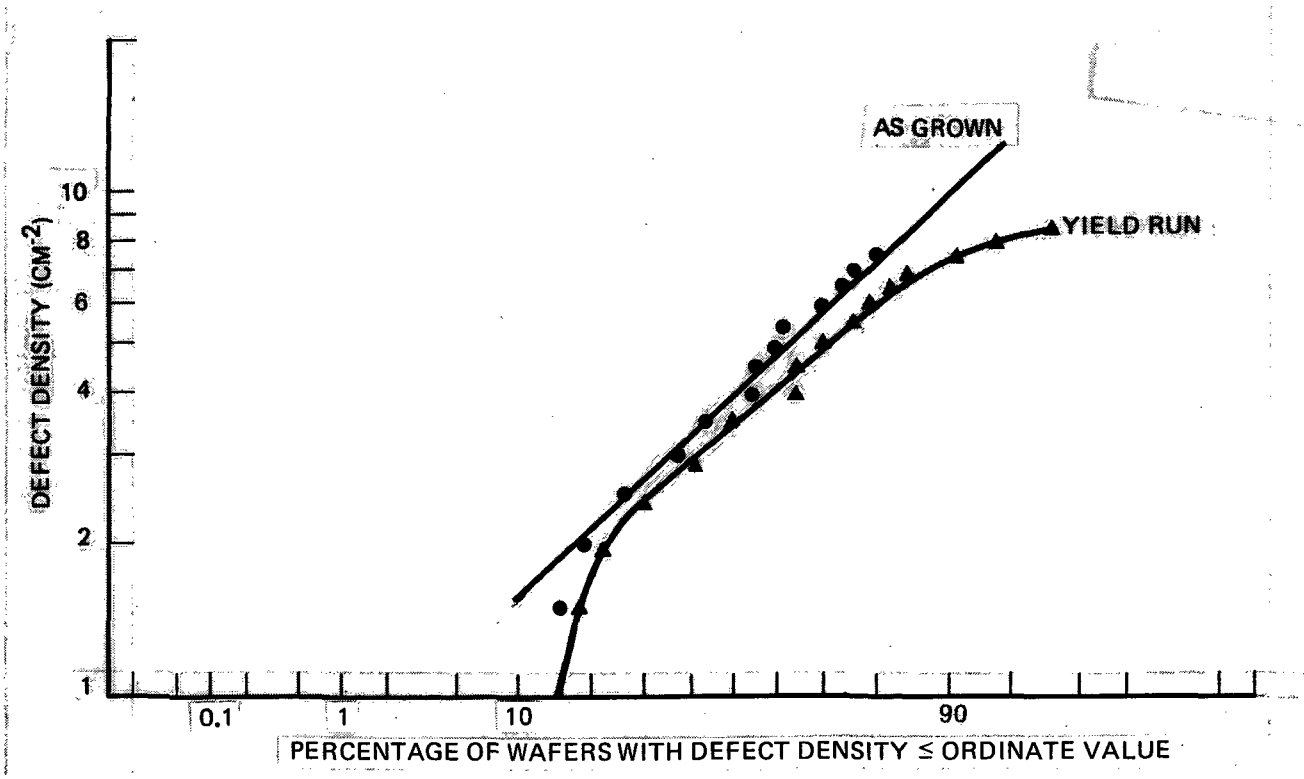


Figure 36. Garnet Defect Density Distribution (for 44 Wafers as Grown and for 32 Wafers as Used in the Second Yield Run)

The new automatic dipping LPE stations had a 3 set point thermal program and each evening at the end of the deposition runs, the temperature automatically was raised to 1150° C briefly and the melt stirred. The objective of this programming was to ensure proper solution of the melt and to improve melt homogeneity. It was found that Pt was being removed from the Pt stirrer and Pt crucible at the high temperature resulting in a higher defect density growth. The auto-dippers were reprogrammed with the original procedure of no stirring and holding the overnight temperature at 50° C above T_{sat}. This solved the high defect density problem. The resultant 44 films (including the two which cracked on cooldown) showed 27 wafers with defect densities ≤ 5 cm^{-2} and 38 wafers <9 cm^{-2}. Six wafers had a defect density ≥ 9 cm^{-2}. One wafer, with $n_g \leq 9$, had too large a stripwidth and could not be used for the yield run. The net result is that 35 wafers were ion implanted and delivered for device processing.

6.2.2.2 Device Fabrication Yield. - The device fabrication run began with 35 wafers. One wafer was broken and two wafers were destroyed by overetching when unacceptable conductor patterns were chemically removed. These two wafers were accidentally left in the etch for several hours and the etch solution attacked the garnet film. The second yield run target values for the device films are shown in Table 16.

TABLE 16. DEVICE PROCESS REQUIREMENTS FOR SECOND YIELD RUN

Parameter	Target Value
SiO_2 Barrier Layer (Sputtered)	900 ±100Å
AlCu Conductor Layer (e-beam evaporated)	4250 ±250Å
SiO_2 Spacer Layer (Sputtered)	5500 ±500Å
NiFe Propagation Layer (Sputtered)	3250 ±250Å

The second yield run showed significant improvement in the ability to hit the targeted film thicknesses within tolerance limits. Table 17 shows the individual layers, the range of thicknesses achieved and the number of runs which exceeded the target tolerance values.

TABLE 17. DEVICE PROCESS FILM THICKNESS RESULTS

	Low Value	High Value	Deposition Runs	No. Out Of Tolerance	
				Low	High
SiO_2 Barrier	800Å	1000Å	11	ø	ø
AlCu	4000Å	5000Å	11	ø	1
SiO_2 Spacer	4500Å	6200Å	12	1	2
NiFe	3100Å	3500Å	13	ø	ø

The improvement of deposition control of the device film thicknesses is readily apparent. The single AlCu film which was out of specification occurred because the deposition thickness monitor (quartz disc) was overloaded with deposit and did not give a correct reading. In ordinary production process control, this probably would not have occurred. The SiO_2 spacer film continues to be the least controllable deposition parameter. The major contribution to the variation of this sputtered film is probably due to the long deposition time (>150 min) over which the random drift of preset deposition variables affects the time averaged deposition rate. The control of the magnetic and electrical properties of the NiFe and AlCu films was very good with results similar to that achieved in the first yield run.

The second yield run device design included reduction of the linewidth and gapwidth values. The second yield run device pattern (M-1061) had a basic 2.2 μm linewidth and a 1.0 μm gapwidth design. The results of the measurement on the processed devices showed a significant improvement over the first yield run. The range of the measured ratio of linewidth to gapwidth was 1.8 to 2.6. This is to be compared with the designed ratio of 2.2. The average value was ~2.2. These results showed a significant improvement in photolithography pattern geometry control, from the first yield run.

The garnet film characteristics of the wafers selected for device processing are shown in Table 18. The mean value of the selected film characteristics does not deviate too much from the full LPE film set, however, the standard deviation is significantly less for the select population, with the exception of defect density.

6.2.2.3 In-Process Testing Yield. - The first version of the Rockwell bubble device wafer prober (Ref 26) was operational during the second yield run. Testing on this version of the wafer prober was based on requiring a good device to have a propagation margin of ≥6 Oe during continuous propagation at 100 kHz. The detected signal was

TABLE 18. GARNET FILM CHARACTERISTICS OF THE WAFERS PROCESSED WITH DEVICES

	Mean Value	Standard Deviation	
		Abs	%
Film Thickness	3.42 μm	0.117	3.4
Strip Width	4.05 μm	0.167	4.1
Collapse Field	110.76 Oe	8.92	8.1
Saturation Magnetization	243.3 Oe	11.85	4.9
Defect Density	3.96 cm^{-2}	2.18	55.1

displayed on an oscilloscope and the propagation margin determined to be the range of pattern stability while the bias field was manually varied. The generator and annihilator were not activated during this test. This mode of testing was considerably faster and less hazardous to the devices than visual/gated mode testing. In addition, this mode enabled a more quantitative definition of goodness. A good device was defined as one which had a minimum 6 Oersted bias margin at room temperature. Table 19 shows the basic results of this in-process testing. For completeness of data, those devices which had a probe margin less than 6 Oe are listed also. This will enable comparison of yield results, on an equal basis, with the first yield run and also permit an accurate yield computation to a more realistic test requirement of a minimum 6 Oe margin.

Three of the 35 wafers selected for device processing were broken or damaged through loss of ion implant layer before they had progressed to the high resolution lithography steps. These wafers will not be included in the statistics. Wafer No. 8-2-21 had 6 good devices at wafer probe its first time through, however, it was discovered that the propagation pattern had been over milled. The act of "overmilling" the propagation results in excessive milling of the oxide which covers the sloped walls of the conductor. When the overmilling is excessive, the oxide can be removed sufficiently to expose the conductor material. When subsequent photoresist mask layers are developed (with a basic pH solution) the conductor (Al/Cu) material is chemically attacked. In this instance, the overmilling and resultant etching of the Al/Cu was sufficient to require rework of the wafer. This wafer was reprocessed, hence it is counted twice in the statistics. This accounting amounts to 33 wafers to be used in the statistics of the yield run. If we again assume an average photomask yield of ~85 percent over the course of the processing (estimated as a result of periodic mask inspection), the maximum possible number of good patterns is 365 dice. On the basis of in-process testing requirements analogous to the first yield run (but not exact since the first yield run wafer test was 25 kHz gated visual), the fabrication process yield is at least 17.8 percent (65/365). The actual process yield to the 6 Oe minimum requirement is 12.9 percent (47/365). The yield at the individual dice characterization point is 7.7 percent (28/365) as shown in Table 19.

For purposes of direct comparison the defect density of each wafer is listed in Table 19. Notice that only two wafers (8-2-6 and 8-2-16) with defect densities >4 cm^{-2} produced good devices at wafer probe. The defect map of one of these wafers (8-2-16) showed that the defects were clustered into the wafer center and only covered two dice locations. This wafer (8-2-16) had five good dice. Its effective defect density is obviously much less than the listed 6.5 cm^{-2}. The point to observe from Table 19 is that the 23 wafers (254 potential dice) with defect densities ≤ 4.0 cm^{-2} produced 45 good wafer probe tested dice. If these wafers had been used solely for the yield run, according to initial specification, the wafer probe yield would have been 17.7 percent and the characterized dice yield would have been 10.6 percent. The importance of the garnet defect density requirement is amply demonstrated from these data.

The wafers were visually inspected microscopically after wafer probing and each die inventoried for its defect count according to defect type. The results are shown in Table 20. Also included in Table 20 are the same data for the first yield run. As was noted for the first yield run, there were permissible minor pattern defects on a good die hence the visual yield is less than the operable dice probe yield. Notice that from Table 20 that the visual inspection accounting yield (15 percent) agrees better with the wafer probe yield for all operational devices (17.8 percent) when compared to the first yield run visual inspection yield (15.7 percent) and the wafer

TABLE 19. WAFER PROBE AND DICE CHARACTERIZATION RESULTS FOR THE SECOND YIELD RUN

Wafer I. D.	Wafer Probe Margin (100 kHz) No Dice <6, Oe	No Dice ≥6 Oe	Wafer Defect Density	Dice Characterization Results (150 kHz)	#	Remarks	Post Probe Damage Service (#)
8-1-2*	—	—	1.0	—	0	Processed 3 times — Wafer broken in processing	
8-1-3	0	3	4.0	15 Oe	1	1 Good die damaged during dice and break operation	Dicing (1)
8-1-4*	0	0	1.0	— *	0	Processed 5 times — Zero good devices — stripped for garnet defect mapping	
8-1-9*	1	1	1.0	10 Oe	1	Processed twice	
8-2-3	0	1	3.6	—	0	Good die damaged in dicing	Dicing (1)
8-2-6	1	2	7.5	8 Oe	1	1 Die damaged after probing	Handling (1)
8-2-7	—	—	2.5	—	0	Wafer broken in processing	
8-2-8*	0	2	4.0	8 Oe, 12 Oe	2	Processed twice	
8-2-9	1	2	3.6	7 Oe, 8 Oe	2		
8-2-10*	0	1	1.2	7 Oe	1	Processed 3 times	
8-2-11	1	0	6.0	—	0		
8-2-12*	0	4	3.6	—	0	Wafer totally destroyed during break operation — Processed twice	Dicing (4)
8-2-13	0	0	7.3	—	0		
8-2-14	0	0	8.6	—	0	Patterned wafer shipped to LRC	
8-2-16	1	5	5.6	7 Oe, 8 Oe, 9 Oe, 10 Oe, 12 Oe	5	Defects actually clustered — no good devices in cluster area	
8-2-17	0	0	7.8	—	0	Patterned wafer shipped to LRC	
8-2-18	—	—	5.0		0	Wafer broken in process	
8-2-19	3	2	1.0	7 Oe, 11 Oe	2		
‡ 8-2-21*	3	3	2.7	—	0	Wafer overmilled — Reprocessed — no good devices	Rework (3)
8-2-22	5	4	3.1	8 Oe, 11 Oe, 17 Oe	3	1 Good die damaged in dice and break	Dicing (1)
8-2-23	2	1	3.4	9 Oe	1		
8-2-25	0	0	5.8		0	Lost inplant due to over conductor etch	
8-2-26	0	2	2.9	13 Oe	1	1 Die unstable after dicing — Damaged after probing	Handling (1)
5-9-27	0	3	3.7	6 Oe	1	2 Dice damaged after probing	Handling (2)
8-2-29	0	1	2.3	7 Oe	1		
8-2-30	0	2	2.6	12 Oe	1	1 Die damaged in dicing	Dicing (1)
8-2-31	0	0	6.5		0	NOT DICED	
8-2-32	0	2	3.0	9 Oe, 12 Oe	2	1 Die damaged during oxide etch	Oxide Etch (1)
8-2-33	0	0	5.5		0	NOT DICED	
8-2-34	0	0	5.6		0	Lost inplant NOT DICED	
8-2-35	0	0	5.0		0	NOT DICED	
8-2-36	0	2	2.5	11 Oe, 12 Oe	2	X	
8-2-27	0	0	6.8		0	NOT DICED	
8-2-38	0	1	1.0	7 Oe	1	X	
8-2-39	0	3	2.0		0	2 Dice lost — faulty break path after scribing, 3rd had less than 6 Oe margin	Dicing (3)
‡ 8-2-21	0	0	2.7		0	Reprocessed due to overmilling 1st time (‡) all dice bad.	
Totals	18	47			28		

TABLE 20. SECOND YIELD RUN DEFECT DISTRIBUTION BY TYPE AND FREQUENCY OF OCCURRENCE

Defect Type	Run #1 / Run #2	Percentage of Dice with n Defects							
		0	1	2	3	4	5	6	≥ 7
Garnet	#1	64.8	22.4	7.5	4.4	0.9	-	-	-
	#2	68.3	20.3	9.0	2.0	0.4			
SiO_2	#1	86.0	11.1	2.0	0.6	0.3	-	-	-
	#2	80.8	14.6	3.5	1.1		-	-	-
Conductor	#1	83.8	13.9	1.7	0.6	-	-	-	-
	#2	88.3	10.4	1.3					
Permalloy	#1	88.9	9.4	1.4	0.3	-	-	-	-
	#2	91.3	5.6	1.9	0.5	0.2			
Photolithography	#1	49.1	28.9	13.9	4.9	1.2	1.2	0.3	0.5
	#2	46.8	30.3	14.5	6.0	1.4	0.6	0.4	
Ion Milling	#1	95.7	4.3	-	-	-	-	-	-
	#2	95.0	4.4	0.4	0.2				
Post Fabrication Handling, Dicing, Mounting, Etc.	#1	80.5	16.9	2.0	0.6	-	-	-	-
	#2	75.8	14.3	4.2	3.0				
Percentage of Dice with ≤ n Defects	#1	15.7	62.4	85.0	95.6	98.0	99.5	99.7	100.0
	#2	15.0	55.8	84.6	96.5	98.8	100.0		
Average of #1 and #2		15.3	59.1	84.8	96.0	98.4	99.4	99.7	100.0

level test yield (11.4 percent), and this in spite of the fact that the test procedure for the second yield run was more quantitative than the first. Probably the principal conclusion that can be drawn from the visual inspection yield data is that we became more proficient at inspecting for visual defects over the time span of the two yield runs.

These data for the visual defect inventory have been summarized for each yield run at bottom of Table 20. Since we are dealing with random defect modelling, (notice that neither of these data sets include handling or dicing or mounting and bonding defects after wafer test), it is instructive to look at the distribution of the numbers of defects, of all types per die i.e., the probability function for 0, 1, 2 etc. defects per die. The data points for each yield run have been plotted in Figure 37 on a log probability plot. Also shown in Figure 37 is the product of the yield terms, Y_G and Y_C as computed using the form:

$$Y_T(n) = \sum_{i=o}^{n} \left(\frac{\lambda_G^{n-i} \; e^{-\lambda_G}}{(n-i)!} \right) \cdot \left(\frac{\lambda_c^{i} \; e^{-\lambda_c}}{i!} \right) \qquad (13)$$

where λ_G is given by Eq (6) with $n_g = 4 \text{ cm}^{-2}$

λ_C is given by Eq (7) with $n_c = 4.1 \text{ cm}^{-2}$

$\lambda_T(n)$ is the probability of having n total defects in a 100K bit die when the garnet and circuit defects are added together.

There are two salient points to be made about these probability curves. First note that the curve for the sum of the defect data of yield runs 1 and 2 (reasonable since the probability differences at each defect value are small) forms a log normal distribution, i.e., a straight line similar to the straight line plot shown by the plot of Eq (13). In effect this verifies our assumption of a Poisson yield model. Point two is that the data curve does not directly overlay the Eq (13) plot, hence the defect density values are different. If we assume that the garnet defect density used in Eq (13) is correct, i.e., $n_g = 4 \text{ cm}^{-2}$, the yield data curve requires a value of $\sim 7 \text{ cm}^{-2}$ for n_c, the circuit defect density instead of the calculated value of 4.1 cm^{-2}. The near agreement of the n_c values provides further confidence in the model.

The agreement, in form, for the defect distribution of the yield runs with the proposed yield is most satisfying. This agreement is strengthened by the fact that the sample size constituting the data which forms the yield run defect distribution amounts to more than 700 dice.

6.2.2.4 Post Fabrication Process Yield. - After the dice had been wafer probed, they were scribed with a CO_2 laser and broken with a typical roller breaker used for semiconductor wafer breaking. Many good dice were damaged either through wafer or dice handling in the wafer dicing, die mount and wire bond process operations after wafer probe. Fifteen dice as listed in Table 19 were damaged between the wafer probe and mounted die steps. This amounts to a yield for this segment of device processing of only 68 percent. The principal reason for these large number of dice losses in wafer dicing was the unfamiliarity with the use of the CO_2 laser scriber to scribe garnet wafers. The CO_2 laser scribe is performed by lasing the wafer on the

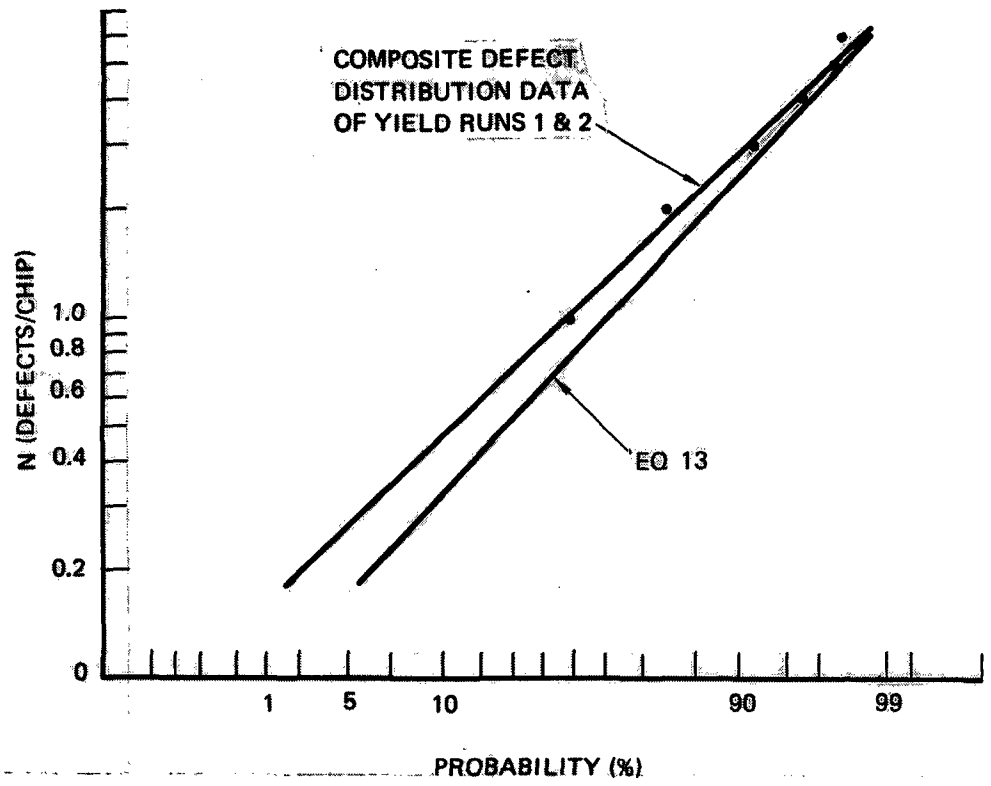


Figure 37. Probability of Finding ≤N Defects on a Chip

backside, followed by a break operation similar to semiconductor wafer technology. The path of the break plane through the wafer occasionally does not travel in a plane normal to the wafer surface. The break plane would occasionally cleave through the front surface of a die resulting in a damaged die.

6.2.2.5 Second Yield Run Summary. - The second yield run results by process stage are summarized in Table 21. Although superficially the results summary do not appear to show a large improvement over the results shown in Table 12, the fact is that even with a more restrictive definition of "goodness", the final characterized dice yield exceeded the first yield run by more than 40 percent. Much of this improvement was due to improved chip design and tighter photomask requirements and the balance to an average lower garnet wafer defect density and the benefits of process experience.

TABLE 21. CUMULATIVE PROCESS YIELD VALUES FOR THE SECOND YIELD RUN

Process (Wafer)	Yield	Comments
Polish	0.98	One wafer broken
LPE Film Growth	0.82	1 wafer broken in hot (200°C) etch 4 lost in melt 2 cracked during cool-down 1 large stripwidth
Ion Implantation	0.82	
Characterization	0.70	6 wafers rejected for defect density >9 cm^{-2}
Process (Device)		
Wafer Fabrication	0.91	1 wafer broken 2 wafers over etched-lost implant
In-Process Testing (Wafer Prober)	0.13	47 Good devices out of 354 possible with ≥6 Oe margin at 100 kHz
Visual Inspection	0.15 ‡	Includes garnet defect density n_g, as well as circuit fabrication defect density, n_c.
Post Fabrication	0.077	Dice characterized for ≥6 Oe margin at 150 kHz. 28 good dice.

‡ See discussion in Para 6.2.1.3.

The 150 kHz operating margin data for the characterized devices are shown in Figure 38.

6.2.3 Third Yield Run. - What is called the third yield run in reality was a program task to start and process as many wafers as were deemed necessary to fabricate a sufficient amount of dice to form nine sets of matched memory elements with eight 100K bit devices per set. The analyses of the first two yield runs identified the remaining yield loss sources in the wafer and device fabrication technologies. The process modifications made after the second yield run were minimal. More stringent criteria were applied to the definition of a "good" device and tighter controls were placed on the garnet exptaxial parameters and defect density. In addition, the third yield run used 2.0 in. diameter wafers which result in ~34 potentially good dice/wafer. The photomask array was increased to a 7x7 size and a new (M - 1067) 100K bit design was used. The photomasks were fabricated on nonreflecting chrome (black chrome) for this run whereas iron oxide masks had been used for the first two yield runs. The fabrication process results analyses for this run were not as extensive as was done in runs No. 1 and No. 2 However, the yield results for this run were significantly improved over the first two runs by any judgement criteria.

6.2.3.1 Third Yield Run Wafer Processing. - The wafer process yield results reported in this section were originally an integral part of the third yield run. However, during the device processing of these wafers, it was discovered that the flatness of these polished wafers did not meet our procurement specifications. Intimate contact between mask and wafer was not adequate to achieve uniform pattern resolution over the 2 in. wafer diameter area, for most of the wafers. A fire in the device process clean room facility destroyed most of the remaining flatter wafers. The data on this wafer run of 65 wafers is included here for the sake of completeness and to show the degree to which the wafer processing has matured in both wafer parameter control and overall wafer yield.

Over the extended period of the garnet film growth portion of this program, the GGG substrate processing was altered to a considerable extent. At the start of the project, 1.5 in. dia material was just becoming available but the polish quality provided by the vendors was unacceptable for device yield goals. However, by the time the final garnet film growth was done on the project, 2.0 in. dia GGG was available from several of the vendors and their ability to provide good quality polished surfaces had improved to the point that high quality low defect LPE films could be grown on vendor-polished wafers.

In the third fabrication run 65 vendor-polished substrates were committed to film growth. Each substrate was cleaned and then etched in 1:1 H_2SO_4:H_3PO_4 at 200° C for 2 min. This was done to delineate substrate defects, such as dislocations and scratches and also to remove any possible residual polishing damage. Each substrate was then inspected optically at 110X.

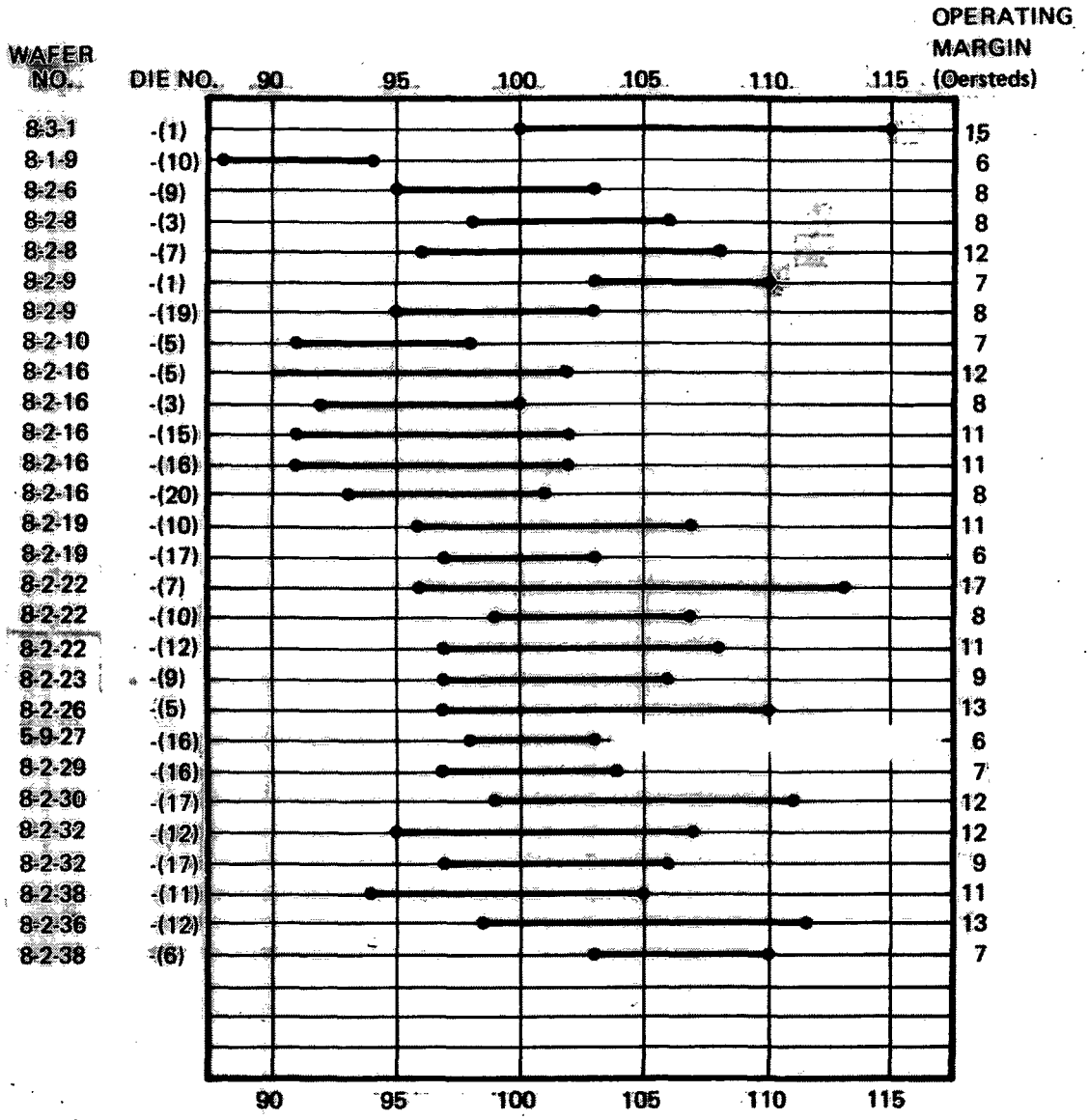


Figure 38. Bias Margins for Second Yield Run Devices. (Conditions: 150 kHz Multiple Bit Pattern, 25°C Drive Field = 50 Oe)

Of the 65 wafers committed to film growth, only one was lost due to breakage. A microcrack or edge chip was thought to be responsible for this loss. The LPE growth was done with the same melt-furnace configuration used for the earlier work. The platinum-5 percent gold alloy wafer growth holder was modified to accommodate the larger 2.0 in. dia material and most of the films were grown one at a time, however eight of the films were grown two at a time in the back to back configuration.

The resultant film thickness uniformity for 2.0 in. dia material was improved over that of the 1.5 in. wafers. The interference fringes indicative of increased thickness at the edge of the wafer were closer spaced and included a narrower band around the wafer than the 1.5 in. dia films. The single fringe (0.13μm/fringe) area of the 2.0 in. dia films had a diameter of 1.75 in. or 76.5 percent of the total wafer area. Film growth yield is here defined as garnet films with defect densities ≤4 per cm^2, film thickness and zero field stripe widths as indicated in Table 22 with collapse field (H_{coll}) value groupings (±1 Oe) such that the resulting devices can be operated in matched groups of eight in a common bias field.

TABLE 22. GARNET FILM SPECIFICATION & YIELD (65 FILMS GROWN)

	Film Thickness (h)	Zero Field Stripe Width (w)	Film Defect Density (75% of area)
Specification	3.15 ±0.25μm	3.65 ±0.25μm	≤4/cm^2
Yield	97%	100%	92%

Of the films grown, seven groups, with H_{coll} values of ±1 Oe were obtained. The group populations were 4, 7, 8, 8, 9, 11 and 12 films for a total of 59 films or 91 percent of the total. Using this yield value and those shown in Table 22 would result in a cumulative yield of 79.6 percent including the one broken wafer. However, one film had two causes for rejection and the actual yield was 81.2 percent. Table 23 gives the mean, standard deviation and maximum and minimum values of the important physical and magnetic film parameters.

The 50 wafer group which was actually used for this fabrication run, as a substitute for the loss of the original wafers, did not constitute a total wafer run by itself. These 50 wafers were a subset of a larger group (~160 wafers) and were selected according to collapse field and stripwidth. The parameter values of these wafers are shown in Table 24.

6.2.3.2 Device Processing. - The device process technology for the third yield run was essentially identical to the second yield run, with two notable differences. The device design was quite different (Type M-1067) and the SiO_2 spacer thickness was reduced significantly. The device process target thicknesses and achieved results are shown in Table 25. Notice from this table that the sputter deposited SiO_2 spacer thickness is still presenting control problems, although the range of the deposited thicknesses is not as large as in the previous yield runs.

TABLE 23. FILM PARAMETERS FOR WAFERS OF TABLE 22.

Parameter	Mean.	Std. Dev.	Max.	Min.
h (μm)	3.060	0.130	3.380	2.710
W_s (μm)	3.650	0.067	3.800	3.500
H_{coll} (Oe)	105.900	5.350	121.100	95.600
σ_ω (ergs/cm^2)	0.193	0.018	0.230	0.160
$4\pi M_s$ (Gauss)	234.700	10.170	256.000	216.000
ℓ (μm)	0.440	0.013	0.475	0.400
Defect Density	2.070	1.490	10.600	0.600

TABLE 24. PARAMETER VALUES FOR THIRD YIELD RUN WAFERS

Parameter	Unit	Mean Value	Standard Deviation	Standard Deviation (%)
Collapse Field	Oersteds	109.70	4.00	3.6
Stripwidth	Micrometers	3.72	0.11	3.0
Film Thickness	Micrometers	3.12	0.18	5.8
Defect Density	cm^{-2}	1.42	+1.23 -0.66	-

Three wafers were broken during the device processing and these wafers will not be counted in the yield statistics. It should be noted, however, that the yield figures to be quoted should be multiplied by 0.94 to be entirely accurate in terms of device process yield. The major source of this breakage appears to be the result of micro-cracks which may be present from the wafer slicing and polishing steps.

6.2.3.3 In Process Testing Yield. - All completed wafers were probe tested on the sequencing wafer prober at 100kHz at room temperature. (Para 7.1.1). The testing sequence consisted of writing in a known pattern and using logic detection and error counting while stepping the bias field. A good device is defined, at this stage of testing, as one which had ten (or more) Oe of operating margin. Table 26 shows the results of this testing. Again, in order to make direct comparison with the first and second yield runs, one column of the table shows a count of all operable devices which includes those with margins less than 10 Oe.

TABLE 25. THIRD YIELD RUN DEVICE PROCESS THICKNESS GOALS AND RESULTS

Film	Specified Thickness	No. Runs	Average (Range)	Standard Deviation ($\pm\sigma$)
SiO_2 Barrier Layer	900Å ±100	7	900Å (800 - 1050)	70.7Å
Al/Cu Conductor	4250Å ±250	7	4300Å (4200 - 4500)	107Å
SiO_2 Spacer	4200 ±400	12	4258Å (3900 - 5200)	375Å
NiFe Permalloy	3250 ±250	12	3275Å (3100 -3500)	174Å

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The yield figures shown at the bottom of the table have been adjusted to account for a 76.5 percent mask limited yield as was done in the first two runs. The justification for this can be seen in Figure 39. This is a composite plot of the good dice/site, for device lots 448 and 449, in the mask that was used for fabricating these wafers. A mask pattern array site which did not produce at least one good die in these 16 wafers is assumed to have been a defective pattern in the mask. Note that dice 35, 36 and 37 are not counted as legitimate wafer pattern sites because this is the handling area of the wafer. Only 34 dice sites are counted in this array. Of these, only 26 patterns produced at least one good die with a 100 kHz operating margin ≥10 Oe. This results in a 76.5 percent mask yield. The yield on this run represents a significant improvement over that of yield run No. 2, yet the definition of goodness was more restrictive: 10 Oe with a controlled logic detected word bit pattern compared to ≥6 Oe with a random, visually detected bit pattern.

A new test criteria was applied to these dice for the third yield run. After the "scan" test, to determine the operating margin, those acceptable dice which had operating margins ≥10 Oe were subjected to a more stringent test of error detection margin and temperature operation sequence. Table 26 shows these test results also. The last column lists those dice which passed this test and shows in parentheses, the number of dice which were subjected to the test. (Not all dice were tested by this means due to the fact that some wafers were not diced). The yield figure shown at the bottom of this column is the product of the 19.0 percent (≥10 Oe) yield and the 72.2 percent (sequencer) yield. The dice which passed this test became candidates for use in the memory cells.

6.2.3.4 Post Fabrication Process Yield. - The scribe and break processes for the third yield run were identical to that used in the second yield run. Of these 46 wafers which completed wafer fabrication, data on the post fabrication process exists for 29 wafers. Some wafers were not diced, because they contained too few (<5) good dice (15 wafers) or because their operating margins did not match sufficiently with other dice in the run to warrant dicing at this time (2 wafers). Of those that were diced, there were 317 good dice (at wafer probe). After dicing, the number of good dice was 294. This amounts to a scribe and break yield of ~92.7 percent. This is a large improvement over the second yield run results where the post fabrication process yield was only 68 percent.

6.2.3.5 Third Yield Run Summary. - The improvements in the results of the third yield run compared to the results of the first two runs is dramatic, to say the least. The factors which contribute to these improvements are: (1) lower garnet defect density, (2) a new 100K bit pattern design, and (3) additional device fabrication experience. Only one of the wafers had a garnet defect density >4 cm^{-2} (5.8 cm^{-2}). The reduction in average garnet defect density for the third yield run (1.42 cm^{-2}) vs the second yield run (3.96 cm^{-2}) accounts for a major portion of the yield improvement. This factor plus the improved pattern and improved device fabrication process control result in a significant yield improvement over that of the second yield run.

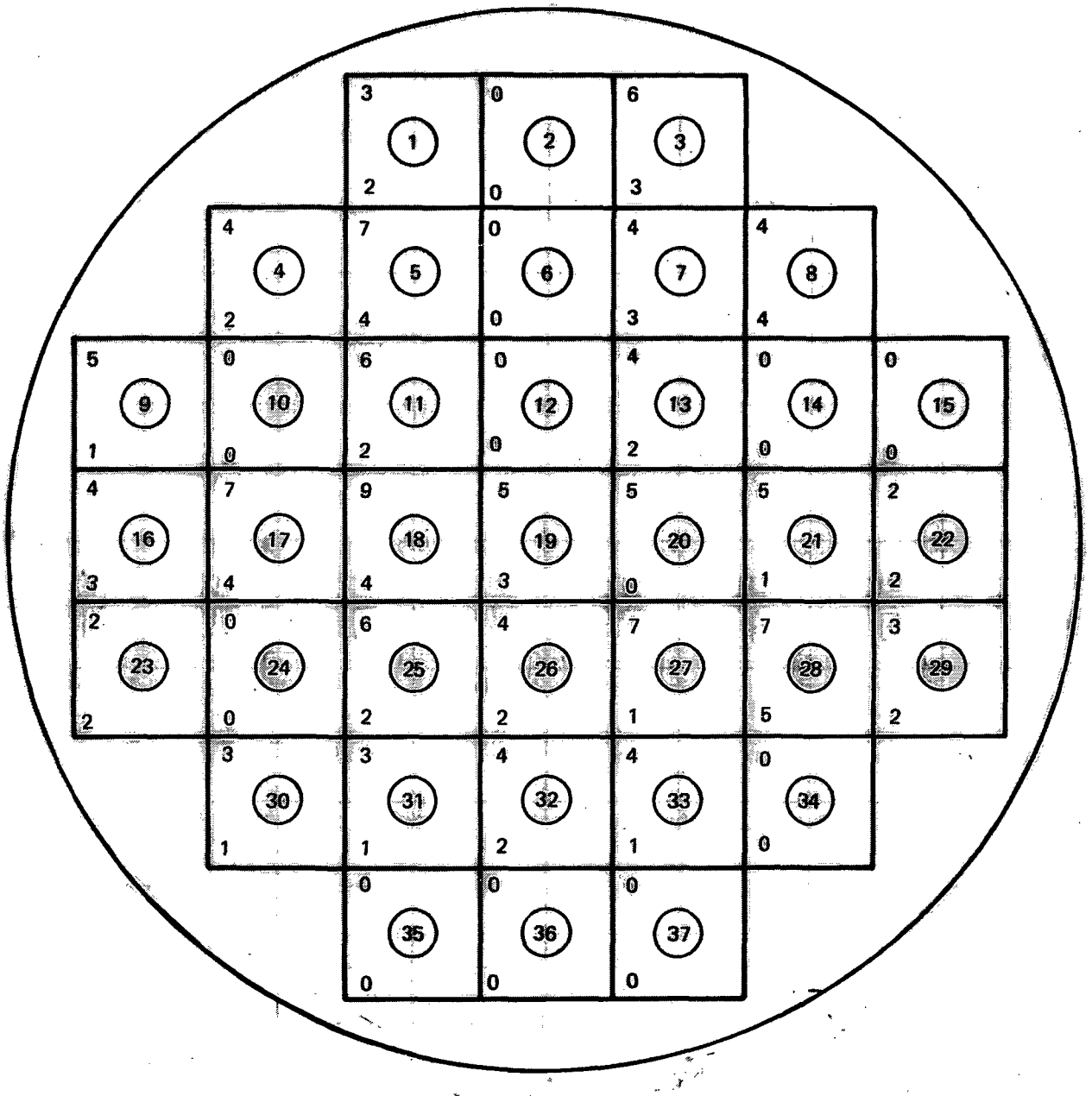


Figure 39. Integrated Yield Results for a 1067 Mask Pattern Array (Process Lots 448 and 449). (The die number is centered on each die site. The integrated number of good dice (≥10 Oe margin) originating from each array point is shown in the upper left corner of each die. The number of dice whose margin is <10 Oe is shown in the lower left.)

6.3 Analysis and Summary of Yield Runs

A summary of these yield runs is shown in Table 27. It should be recognized that the bottom line figure - overall yield does not take into account the increasing restriction on the definition of a good device after the first yield run. Yield run No. 3 shows 130 for the total number of good dice. These are the dice which passed the $30^{o}C/60^{o}C$ combined margin requirements. These are certainly reasonable and necessary requirements for the application contemplated. Probably the most meaningful circuit fabrication yield is the cumulative yield after dicing which deducts for the wafer breakage prior to in-process testing and those patterns which were defective on the working mask.

The three yield runs have proven that the technology needed to fabricate the high resolution (~1 μm), high density ($\geq 10^{6}/cm^{2}$ high resolution features) 16 μm period bubble devices has been developed. The maturation and adaptation of the technology is clearly evident in the results of these yield runs. In spite of an increasingly

TABLE 27. YIELD SUMMARY FOR ALL THREE YIELD RUNS

	Run No. 1	Run No. 2	Run No. 3
A. Wafer Starts	50	50	65
B. Wafer Process Yield	0.660	0.700	0.810
C. Device Fabrication Wafer Starts	33	33	50
D. Mask Limited Yield	0.850	0.850	0.765
E. Potential Dice/Wafer	11	11	26
F. In-Process Test Yield (All Operating Devices)	0.114	0.178	0.338
G. Minimum Performance Yield (Operating Margin)	-	0.129 (≥6 Oe)	0.199 (≥10 Oe)
H. Cumulative Yield through Dicing	0.054	0.077	0.184
I. No. of Operational Devices	19	28	130
J. Overall Yield I/(C·E)	0.052	0.078	0.100*

*Only 29 wafers were diced, 17 wafers with a total of 30 good devices were not diced. Had these experienced the same handling and dicing yield, the overall yield would have been ~0.113, hence 0.10 represents a minimum overall yield.

stringent definition of what constitutes a good device, the yields have shown a continuing increase with each run. The data from Table 20 as plotted in Figure 37 shows a very satisfying correlation with the yield model expressed in Eq (13). This data plot confirms the validity of the model. The results shown in Figure 37 also illustrate a point discussed earlier (Para 2.1.1) i.e., the fabrication yield of a chip with redundancy can be significantly higher than that of a non-redundant one. For example, if the design had been such as to permit accomodation of only three defects, without affecting overall device performance, the fabrication yield could have been in excess of 95 percent. Even when one accounts for defective patterns in the photolithographic mask array, and the handling damage yield, the overall yield conceivably could approach 75 percent.

However, as mentioned earlier, in any given situation, one must evaluate the tradeoffs and decide whether the potential advantage of a higher fabrication yield can actually be realized and whether this advantage will more than offset the additional chip, testing, and system complexity.

In any event, these yield run results clearly demonstrate that it will be possible, in a production mode, to produce an economically competitive, mass memory market directed, bubble domain device.

7. DEVICE CHARACTERIZATION AND TESTING

In this chapter characterization results pertinent to the chip development will be presented with emphasis on the later chip designs such as M-1065 and M-1067. This chapter should be read with frequent reference to Chapter 2. The various measurement techniques employed will be defined and briefly discussed.

Two different levels of device tests were performed on the bubble domain memory elements fabricated on this program: (1) wafer level tests of registers which had completed device processing except for wafer scribe and break, and (2) die level tests of separated chips mounted on single-chip or multi-chip carriers. The wafer level tests were an in-line monitor of process yield and provided the basis for determining whether wafers should be reprocessed or completed through to die mounting and bonding. The die level tests on single-chip carriers provided a detailed evaluation of the performance of the device and its components. Multichip carrier testing was performed on the same equipment used for wafer level test and was used to confirm that chips had not suffered degradation during the assembly steps of scribe, break, and diemount. Both types of testing became more sophisticated through the duration of the program.

All die level tests were made at 150 kHz, the frequency goal for this program. Wafer level data rate was limited by the tester. Many of the measurements were made over -10°C to 60°C the desired operating range with emphasis at 60°C where reliable device operation is most difficult. To evaluate the asynchronous operation requirement many tests were made in the gated mode. As a result of these evaluations improvements were made in virtually every component of the chip.

7.1 Characterization Techniques

7.1.1 Test Appartus Description. The initial wafer level test method employed an open coil capable of accepting a wafer on a carrier. The drive coil had a maximum practical operating frequency of 25 kHz. The full memory transit time for a bubble was in excess of 4 sec for 100K bit registers. Chip evaluation was accomplished using column gated operation wherein the bubble is propagated a full column length to the same position in the next column. In this manner the bubble pattern appears to propagate orthogonal to the column orientation. This method was useful in isolating defects as well as a preliminary performance check. A "good" device at this level was a device in which a bubble could be column gated completely across the register and then gated through the entire register. A single bubble completing transit was sufficient to designate the chip as good and advance it to further testing. Although this technique was performed at a low frequency and lacked sufficient bias field uniformity due to the coil structure, it did provide important qualitative information about the chip performance.

This method was used only on the first yield run. An upgraded wafer test procedure and hardware (a wafer prober) were designed which provided quantitative wafer level data and reduced the test time. This apparatus was used on the second yield run.

This first version of the wafer prober consists of 4 discrete parts; the head, the stage and electronics, the probe card, and device electronics. The head moves vertically to allow placement of the wafer on the stage and provides the mounting and

electrical interface for the probe card. The probe card is fitted with several probes matching the pad pattern of the wafer under test which is held in place by vacuum. Bias and drive field coils are attached to the card which allow vertical visual access to the probe pad interface area. The stage is electronically moved through x, y and ϕ to properly align the probe-pad interface prior to making contact. The stage can then be incrementally indexed from register to register.

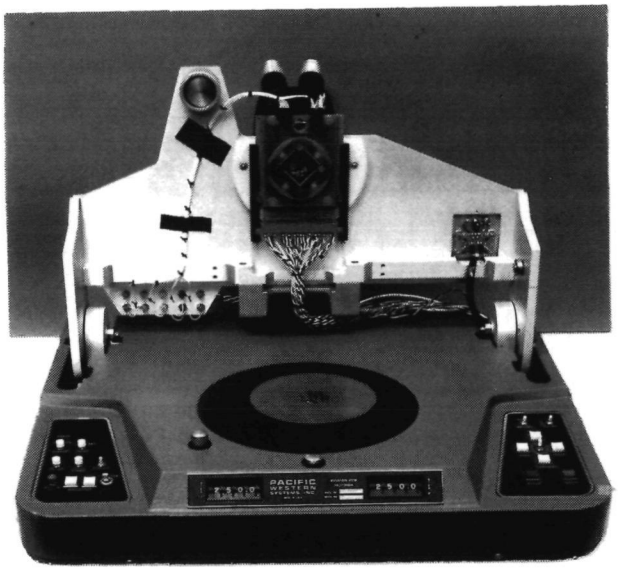
The test electronics employed is a Bubble Domain Memory Exerciser which provides: (1) 100 kHz drive current to the rotating field coils for a maximum drive of 54 Oe, (2) a DC current for the electromagnetic bias field, and (3) Sense electronics and annihilator-generator controls for evaluation of device operation.

This arrangement provides faster, more accurate register evaluation at the wafer level. The actual device margins can be measured and compared to the margins at die level evaluation. A photograph of the wafer prober is shown in Figure 40. This wafer prober was available for the second yield run and Figure 41 shows some typical wafer level to device level margin comparisons. The major reason for differences in margin between wafer test and device test was the lack of temperature control on the wafer prober at that time (T = 30 ± 10°C).

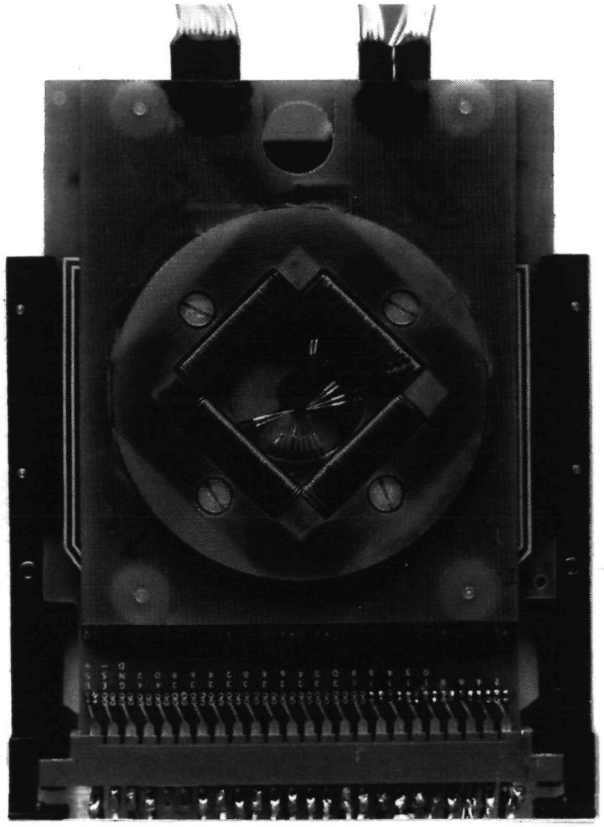
This prober was designed with the capability to write and erase a specific data pattern (through controlled generation/annihilation) and to perform logic level detection of the data pattern. However, due to the absence of temperature control and for expediency in the overall process scheme it was not used in this mode for the second yield run. Rather it was primarily used to measure propagation bias margins by visual observation of an oscilloscope display of the linear detector output. The bias margin for propagation only was determined by observing the field extremes between first disappearance of a bubble signal (collapse) or first emergence of a new signals (stripout or spontaneous generation). The first prober can only be operated in a continuous mode at 100 kHz. A device was considered acceptable if its room ambient propagation margin was ≥6 Oe.

A more advanced version of the wafer prober became available in the later stages of the program which is capable of automatically sequencing through a number of tests. The operating frequency is still limited to 100 kHz but this prober is capable of gated (start/stop) operation as well as continuous. Stage temperature can be adjusted from +25°C to +60°C and maintained at that temperature to within less than 5°C. In automatic operation the exerciser steps the bias field in small increments (~1 Oe) and records the number of errors occurring in the bubble data at each field. Since the margin degradation of bubble chips is about 0.2 oe/decade of propagation steps, about 5 orders difference in error rate will be observed between each bias increment. Thus the error count recorded will vary from >100 errors to 1 or none in only 1 0e. The margin boundaries are determined then when the error count occurs in this range. At this phase of the program a device was considered acceptable when it had an operating margin (gated, 100 kHz, logic detection) of ≥10 0e at 25°C and ≥8 Oe at 60°C. For the YSmGaIG material (Hcoll ~100 Oe) these values correspond to minimum bias margins of ~10% and 8% at 25°C and 60°C.

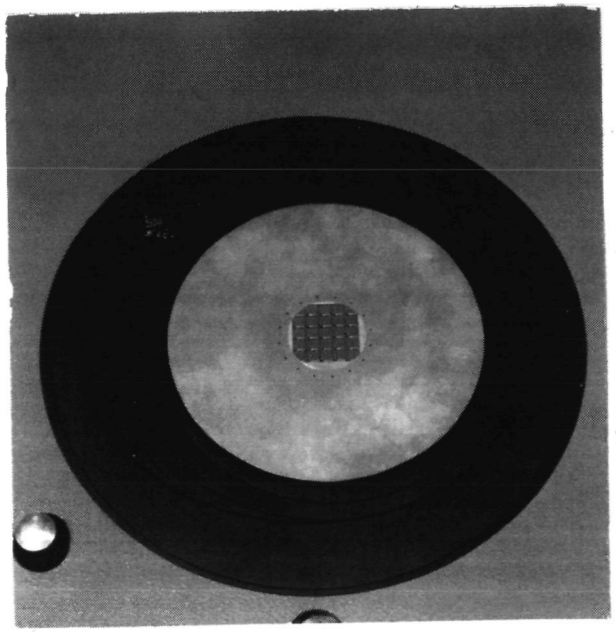
7.1.2 Standard Margin Characterization. - In these measurements a standard Rockwell International bubble domain exerciser was employed with a coil capable of drive fields to 70 0e and with temperature control. Die were mounted on individual test boards for evaluation (Figure 42). Operating margins were measured by varying the dc bias field and the inplane drive field. High end failure is defined by bubble collapse



(a) OVERALL VIEW



(b) PROBES AND ROTATING FIELD COILS



(c) 100K BIT DEVICE WAFER (1.5" DIA.) ON PROBER STAGE

Figure 40. Wafer Prober

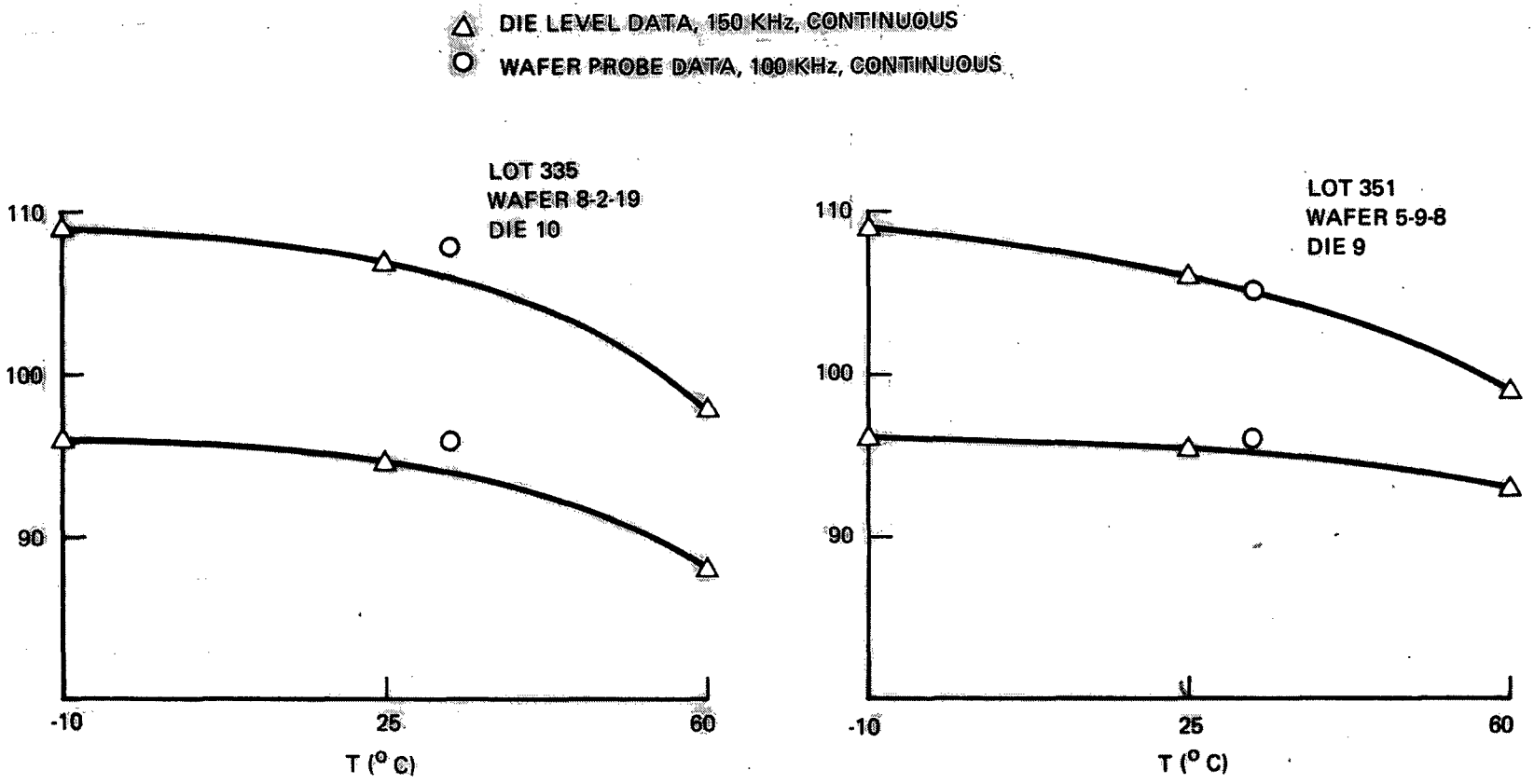


Figure 41. Comparison of the Wafer Probe Margin (T = 30°C) with the Die Level Margin (vs Temperature) for M-1061 Devices

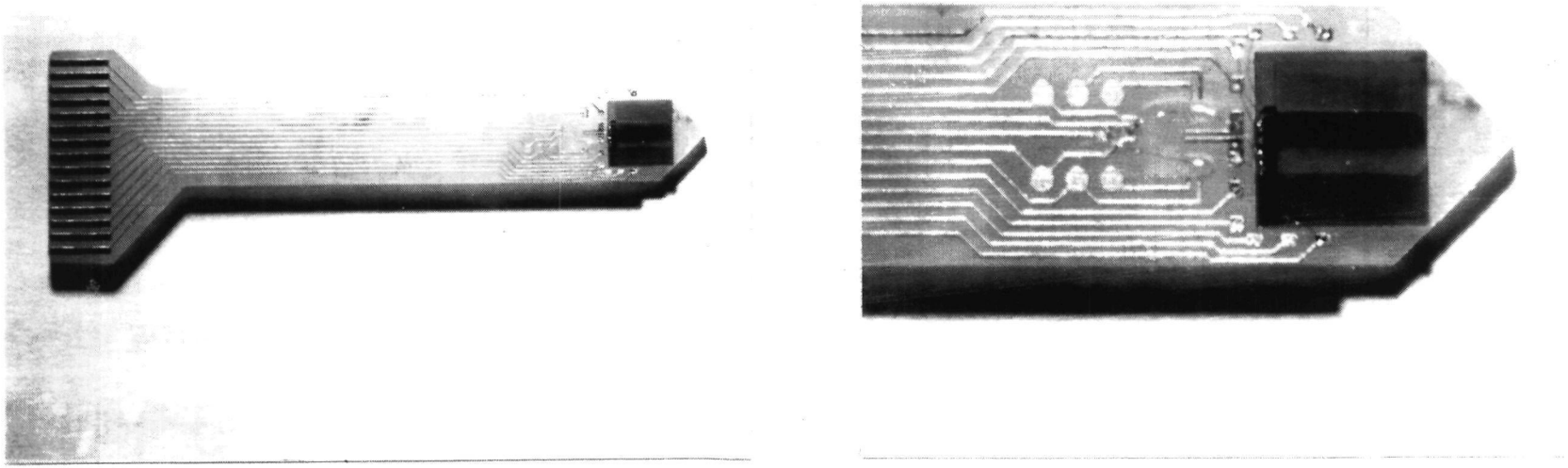


Figure 42. Single Layer Circuit Test Board (Polyamide-Imide Sheathed Epoxy-Glass) (First Version 100K bit Chip Mounted and Bonded)

employing an eight bit pattern containing both adjacent ones and zeros and alternate ones and zeroes. Low end failure was characterized by stripout or additional bits entering the storage. In this case a sparse bit pattern such as (0001000) was employed. The hard error rate for these margin edges were 10^{-6} errors/bit or better. In many cases in addition to propagation the operation of the input and output functions were included in tests. Both continuous and gated tests could be made.

7.1.3 Component Margin Measurement. - The individual propagation components may be evaluated by the field interrupt technique. (Ref 9). Evaluation is accomplished by generating a short data stream which passes through the desired component or location at the time the bias field is shifted from an overall margin center value to a value closer to the component margin edge. After passing through the component the center bias field value is resumed. Typically the data stream is about 80 bits long and the field interrupt pulse is usually somewhat shorter but at least 8 bit times long. Figure 43 illustrates the field interrupt process which can either occur in bias field only, drive field only or a combination.

Before individual components are evaluated it is useful to first identify the weaker components in the device. The device is first filled with a bubble pattern (an all "one" pattern for this example) and operated at the reliable region of the bias margin (Point 0 - Figure 43). A bias field pulse of 80 bits wide is applied in synchronism with memory size so that the whole chip is temporarily at or beyond the top bias margin (Point *o*) for 80 bit times. Within this period, those bubbles propagating through margin limiting elements will begin to fail. By incrementing the bias field range an error pattern picture can be obtained which will clearly show the location of weaker components or even defects.

After the weak components are identified individual component margins can be taken by field interrupt using the short data stream. In this measurement an interrupt pulse is applied for 50 memory cycles at each bias field. Incrementing the bias field until the first error is noted defines the margin edge for that component. Although this only translates to an error rate of only 10^{-3} it still gives the relative margins of each component. It is difficult to measure lower error rates with this particular method because of the comparatively long measurement time.

This measurement technique was only available in the later part of the program.

7.1.4 Long Term Margin Measurements. - This technique, also developed in the latter part of this program, is used to evaluate the long term data reliability of the bubble device. The basic measurement parameter is Mean Step to Failure which is the inverse of the initial failure probability per bit for propagation. This parameter is determined by measuring the accumulation of errors during propagation and extrapolating the initial value of this curve (on a log-log plot) to the point where every bit makes an error. Repeating this measurement at a number of bias fields and plotting the bias field versus MSTF gives the overall margin degradation for that device. MSTF values up to 10^{10} steps can be easily measured by this technique.

7.1.5 Generator and Annihilator Evaluation. - The pertinent parameters for these functions are pulse amplitude, phasing, and pulse width. Margins for these parameters are easily measured in conjunction with the Standard Margin Measurement (para 7.1.2) Annihilation is usually evaluated at the lower bias margin edge which is farthest from collapse. These margins are particularly dependent on temperature.

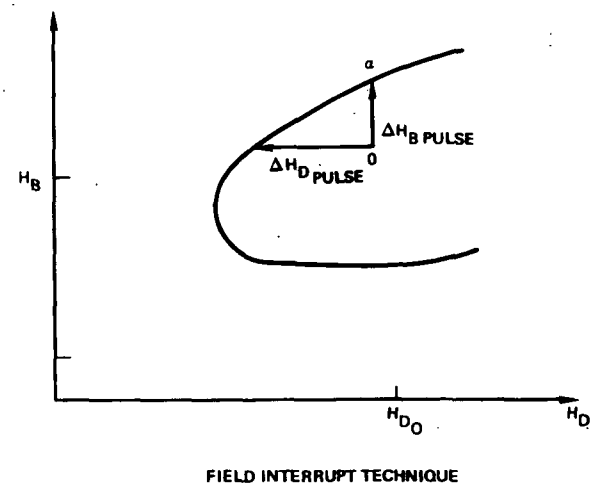


Figure 43. Representation of the Bias (ΔH_B) and Drive (ΔH_D) Field Interrupt Technique (Point 0 is the Normal Operating Point)

7.1.6 Detector Evaluation. - Two measurements used to evaluate detector performance are the "one" and "zero" linear signal with a clamp and the soft error rate versus threshold voltage. The first measurement when made over temperature and inplane drive field amplitude provides data to determine the best unclamp and strobe setting for minimum signal variation, the threshold setting for operation over temperature, and the signal sensitivity. Normally these signals are observed with a standard oscilloscope. Since the signal contains random noise, primarily from domain switching, (and also some systematic noise) the window is defined as the clear region between the "1" and "0" signal. Typically this will correspond to a 10^{-6} soft error rate level. Another important piece of information available here is related to the detector matching on a specific chip. Mismatch will usually result in a large systematic noise component very evident in the "0" signal. Nominally if the "1" to "0" signal level is greater than 8 the mismatch is considered small.

The soft error rate per bit read is determined by measuring the number of read errors occurring over a period of time. Thus

$$\text{ER (soft)} = \frac{\text{Read Errors}}{\text{Bit Read}}$$

Presently, since hard and soft errors cannot be separated the hard error rate must be made much smaller than the soft error rate in order to measure the latter. This is accomplished by setting the bias and drive field at a reliable point. e.g. point 0 in Figure 43. By varying the threshold voltage across the window of a typical one-zero word pattern two curves are generated, one for "zeros" being read as "ones" and the other for "ones" being read as "zeros". For a rough approximation of the signal to noise if it is assumed that each error rate component is Gaussian with the same noise power (i.e. standard deviation) the S/N is given by

$$S/N = 20 \log_{10} \frac{\Delta V_{th}}{2\sigma}$$

where the ΔV_{th} is the threshold window at an error rate of 0.5.

Chip performance in first bit detection can be evaluated by measuring the detector characteristics of that bit or by measuring the operating margin using the standard technique (Para 7.1.2).

7.2 Evaluation of the Various Device Designs

As part of the chip development task and the first and second yield runs, each device was evaluated for its performance. In most every case the standard characteristic margin (Para. 7.1.2) and the generator and annihilator were evaluated. Later in the program when more sophisticated techniques were available these were employed as necessary. Since the performance of the later chip designs is more important to report only pertinent data of the earlier chips will be reported here.

7.2.1 1K Bit Designs. - The device margins for the two level 1K bit design are shown in Figure 44. This design was characterized by high drive field requirements originating primarily from the large design values of linewidth and gap and from the design

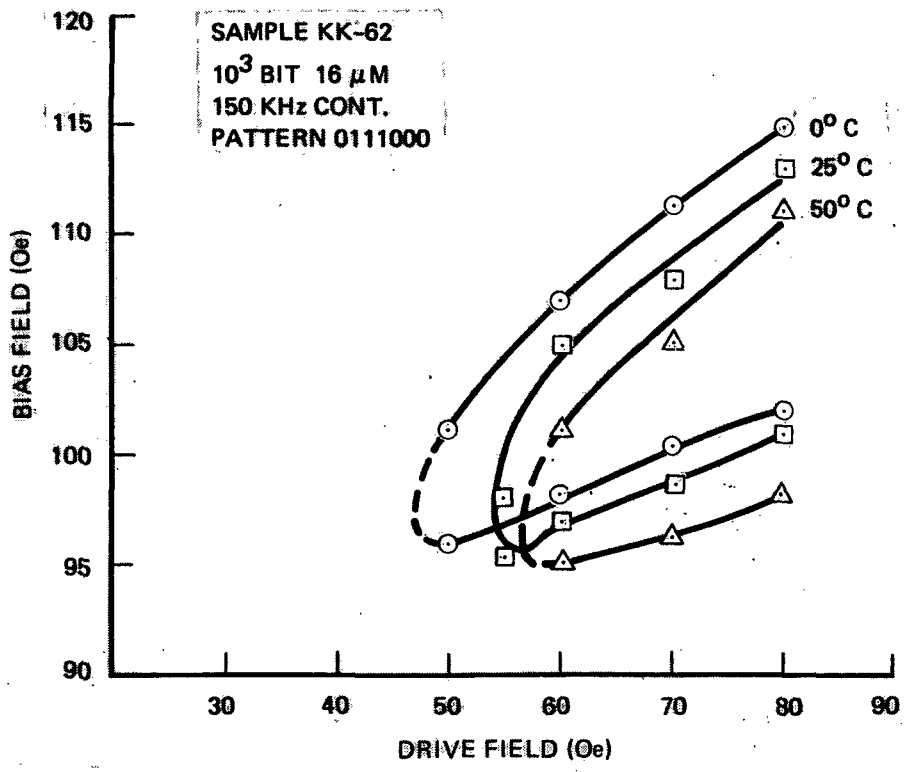


Figure 44. Operating Margins for the 2-Level M-1049 1 K Bit Chip

of the bent-H and X-bar corners. The start/stop characteristics of this design were poor. It was not possible to obtain satisfactory start/stop operation in any direction. These results indicated the need to re-orient the T-bar and chevron regions to improve the reliability of start/stop operation.

The one-level 1K bit device had generally similar characteristics to the two level design but suffered from severe margin degradation and reliability problems associated with the design of the conduction paths of the one level annihilator loop. No further design iterations or evaluations were made on the one level design following the decision early in the program to pursue two level devices.

7.2.2 100K Bit Device M-1050 (First Yield Run). - The first 100K bit design M-1050 was merely an expansion of the two level 1K bit design and had the same performance characteristics, i. e. high drive field requirements, low detector sensitivity and margin degradation for consecutive bit operation. The bias margin of Figure 45 is typical of that observed for the 1K bit chips of this same design. The minimum drive field values were even higher than those for the 1K bit versions because of the additional variations in gaps and the greater likelihood of minor defects in the larger chip area.

At the conclusion of testing on the first yield run, a total of 19 operational devices (any measurable margin) were obtained having margins (single bit) from 3. 5 Oe to 17)e at 80 Oe drive field and 25°C. Analysis of the margin data showed that 17 of these devices could be sorted into three groups (10, 5 and 2) with margin overlaps of 5 to 6 Oe. Annihilator and generator phase plots are shown in Figure 46.

7.2.3 100K Bit Device M-1061 (Second Yield Run). - The design modifications and improvements in fabrication resulted in significantly improved performance. Minimum drives were reduced up to 50 percent and consecutive bit margin doubled at almost half of the drive field. Figure 47 shows a typical gated margin plots for this device. The reduction in minimum drive field is attributed to design changes as described in Chapter 2. The reorientation of the storage region provided considerable improvement in the reliability of start-stop operation when the start/stop direction was along the direction of propagation in the chevron track.

A field interrupt measurement on a 20Kb version of the M-1061 was made to determine the location of the weaker components. Figure 48 shows the results of this measurement for a portion of the device, from the chevron detector to the first T-bar storage column. An error as a result of randomly annihilated bubbles is indicated by a black bar at the bit position where it collapsed. The error pattern for several different bias fields is shown. It can be seen that the weakest component in the chip for the 48 0e drive field used in this case is the T-bar to chevron transition element. Other limiting elements in order of failure are the T-X and Bent-H corners and the detector lead crossover (in-line detector). Total device failure occurs only about 4 Oe above the weak components. Thus these limiting components account for a 20% to 30% degradation in margin.

The generator and annihilator phase margins are normally the same as those for M-1050 shown in Figure 46.

Figure 49 shows the detection error rate for the same M-1061 device as in Figure 47. The error rate and signal sensitivity of M-1061 are much superior to those obtained for M-1050 as a result of the increase in the detector length from 30 elements to 100 elements. The detector sensitivity increased from about 150 μv/mn to 0. 8 mv/ma at 25°C.

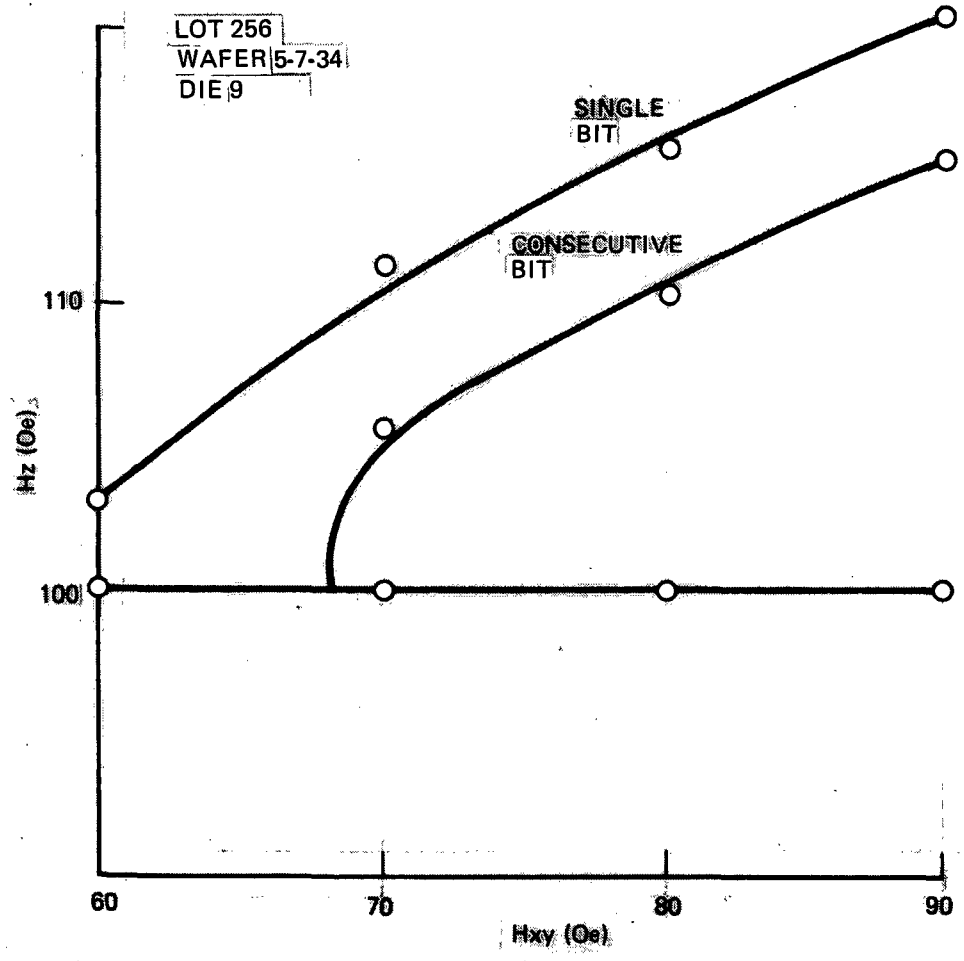


Figure 45. Bias Field Margins (Die Level) for Several M-1050 100K Bit Chips. (1st Yield Run)

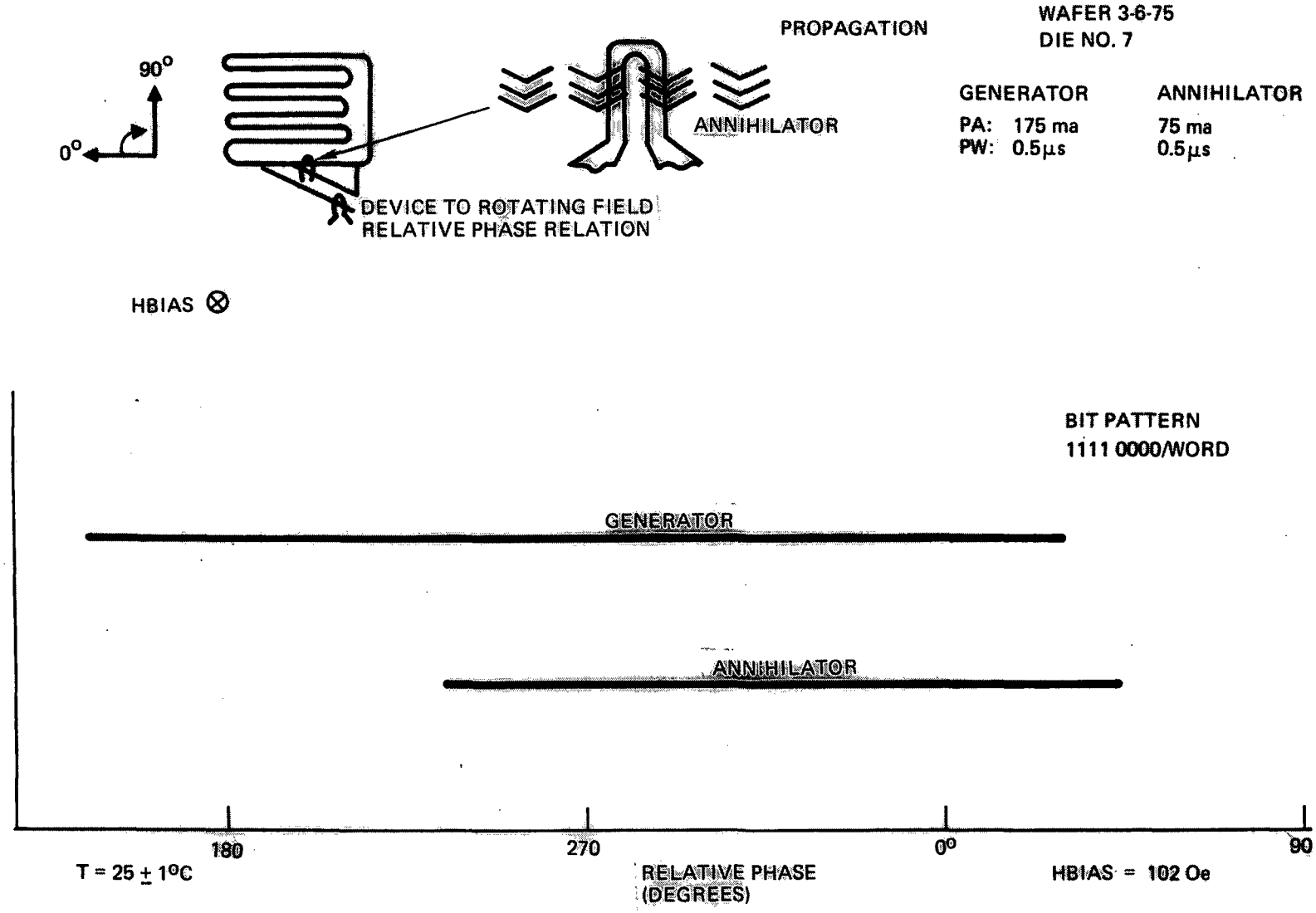
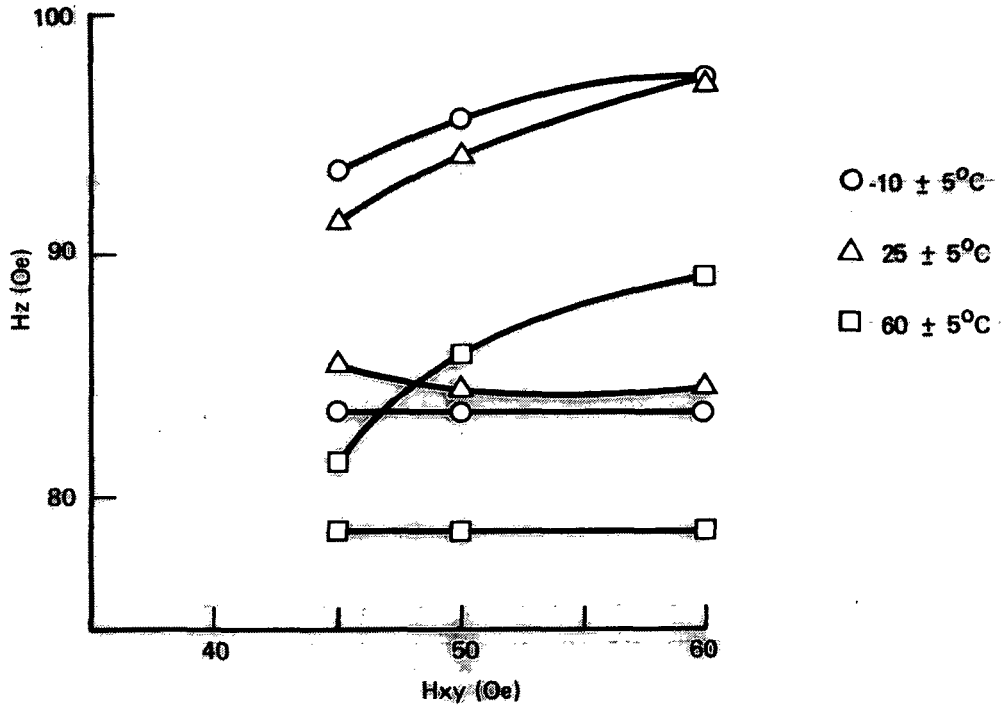
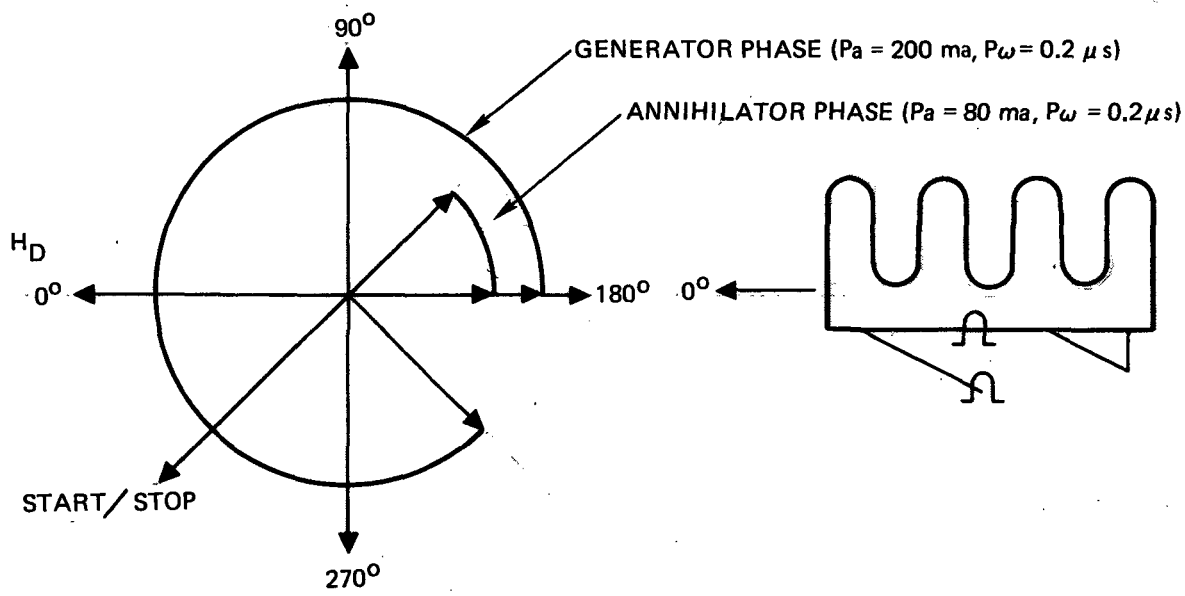


Figure 46. Generator and Annihilator Pulse Phase Margins for M-1050 100K Bit Chip



(a) OPERATING MARGINS FOR THE M-1061 100K BIT CHIP



(b) GENERATOR/ANNIHILATOR PHASE MARGINS

Figure 47. Characteristic of M-1061 Device

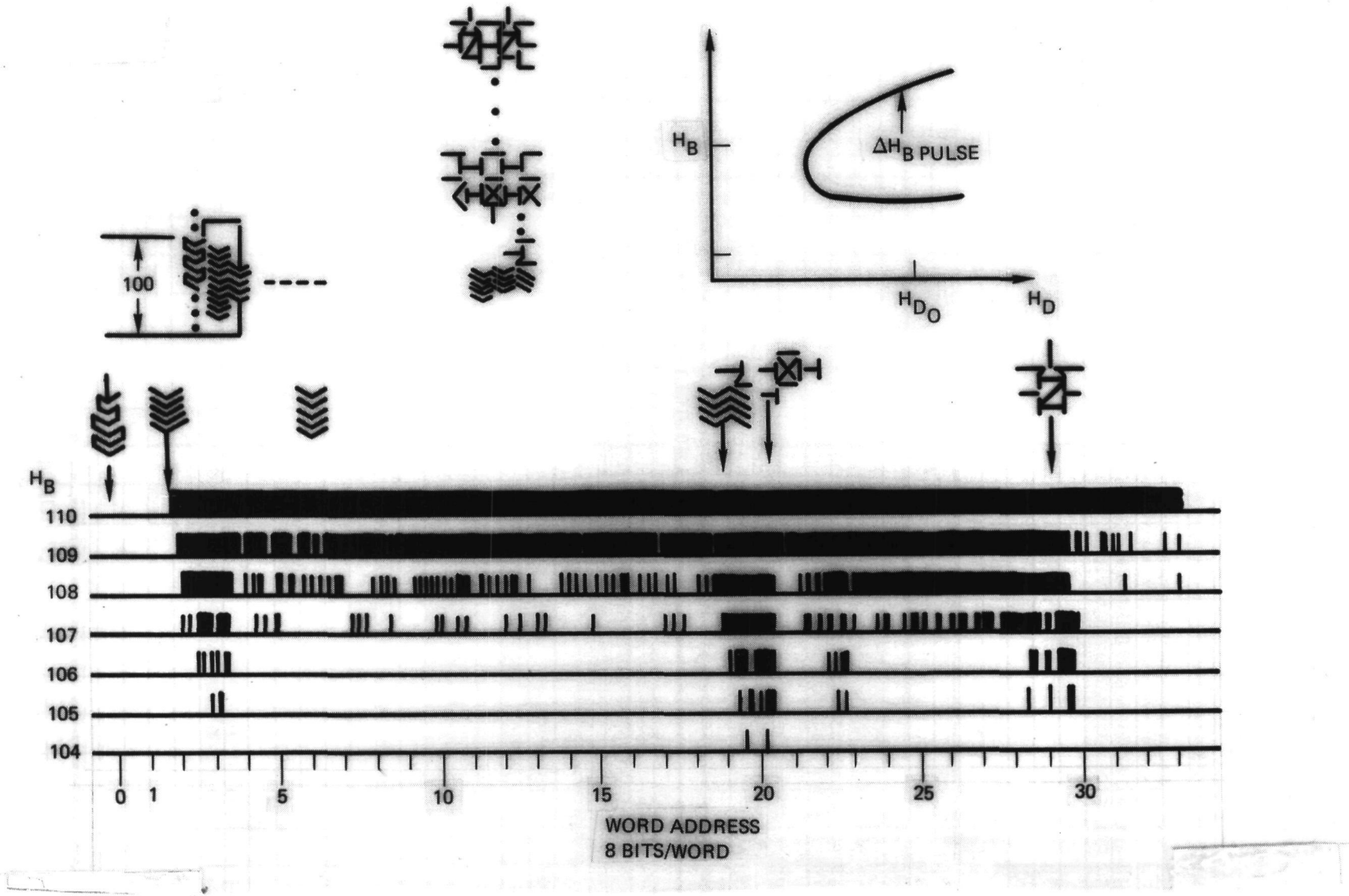


Figure 48. Bias Interrupt Error Scan of a 20K Bit Version of Device. (Center Bias Field $H_B \simeq 100$ Oe)

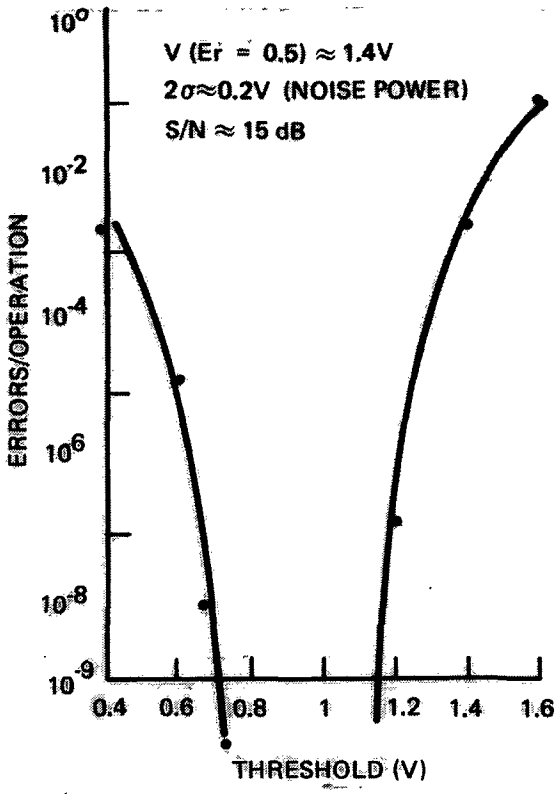


Figure 49. Soft Error Rate for M-1061 Chip. Left Curve is for a "0" read as a "1" and Right Curve is for a "1" Read as a "0"

7.2.4 Final Versions of the 100K Bit Design. - As described in Section 2 there were three device architectures considered for the final memory element design, M-1065, 1066, 1067. The intention of these designs was to further improve device performance by reductions in the gap dimension and refinements in the component designs, to achieve input/output coincidence as in the case of M-1065 and M-1067 and to meet the need for reliable asynchronous operation with first bit read over the operating temperature range. The tradeoffs between the design features of these chips is covered in Section 2, basically they differed only in the input/output regions - the storage areas layout and the component designs were identical.

Version 1066 was intended mainly as a backup chip in case the passive replicator/guardrail detector approach used in 1065 and 1067 proved unacceptable. Since good performance was obtained with the 1065 and 1067 chips, 1066 was never fabricated or evaluated.

The 1065 design was fabricated and characterized and did show the improved performance as anticipated from the design modifications. However, as discussed in Section 2, the reliability for first bit read was expected to be not as good as that of 1067. Consequently the characterization of the latter chip was emphasized and the 1067 design (specifically 1067B with the modified detector feed thru) has been selected for the chips to go into the prototype Solid State Spacecraft Data Recorder design (Contract NAS1-14174).

The bias margin for continuous 150 kHz operation of a typical 1067 device at 30°C and 60°C is shown in Figure 50. For a drive field of 54 0e the bias margins at

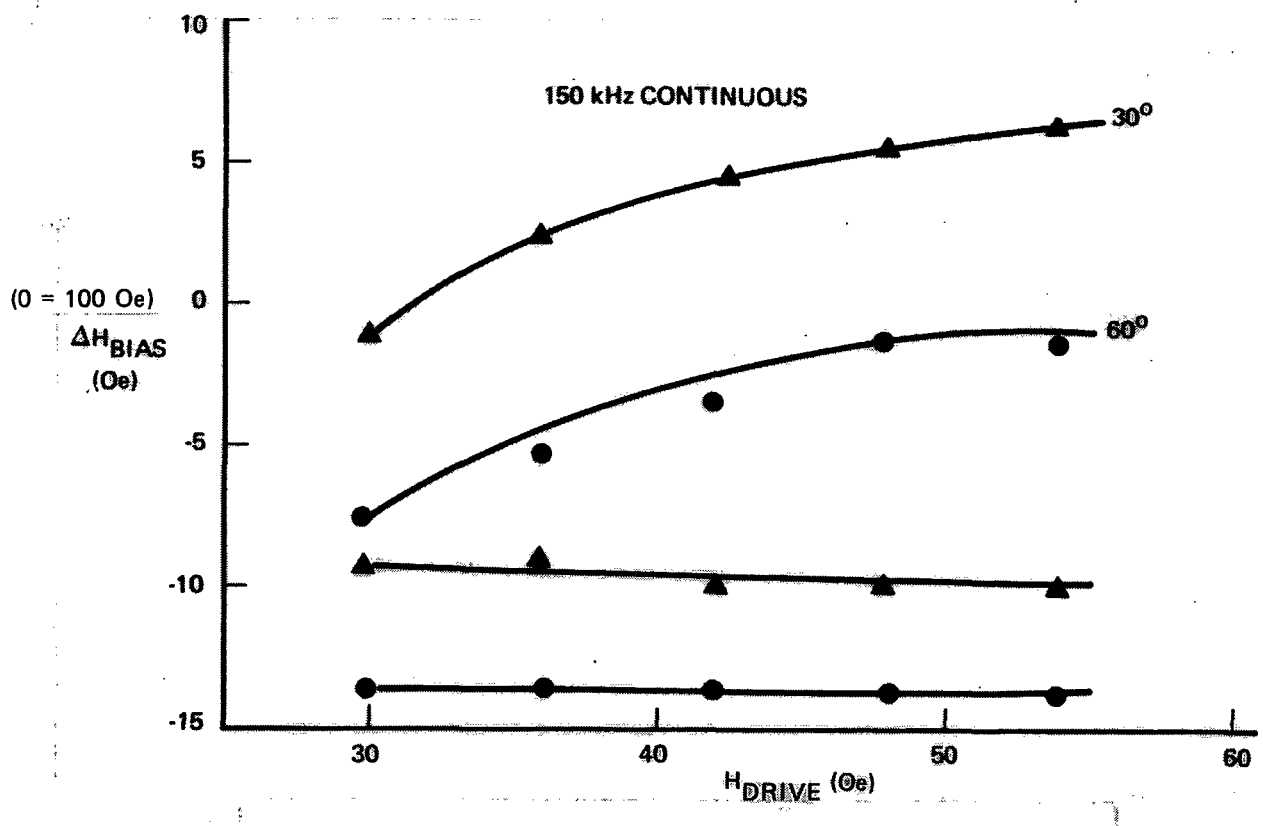


Figure 50. Operating Margin for M-1067B 100K Bit Device

30°C and 60°C are 15 percent and 12 percent respectively. These measurements were performed on a device mounted on a single chip carrier. Comparison of continuous and gated margins for another device in a multichip carrier in an 8-chip memory module is shown in Figure 51. The 30°C bias margin for continuous operation is 12 percent for this device in this cell. It can be seen that the margin for gated first bit detection shows very little degradation from the continuous operation case. Reliable operation with good margins was obtained over the entire temperature range -10°C to +60C.

A long term data reliability measurement in the continuous operation was made on a typical 1067 device using the technique of Ref 9. The results in Figure 52 show that at a MSTF of 10^{11} steps the margin degradation is about 0.2 to 0.3 Oe/decade, a reasonable reliability based on a number of measurements of various device designs.

A component margin measurement by bias field interrupt is shown in Figure 53 for device M-1067. It can be seen that the passive replicator is the component which limits the device margin at the high bias values for low drive fields. The rest of the device components have relatively comparable margin i.e., there does not appear to be any other particularly weak component which significantly limits device performance. The high drive field required to produce ≥10 percent margins for the chip is the price paid for the passive replicator which allows the elimination of delays between the read/write/annihilate functions. It should be noted that the margins in Figure 53 are somewhat larger than the overall device because bit-bit interactions are not considered here and that the error rate of this measurement is higher than that of the standard margin measurement.

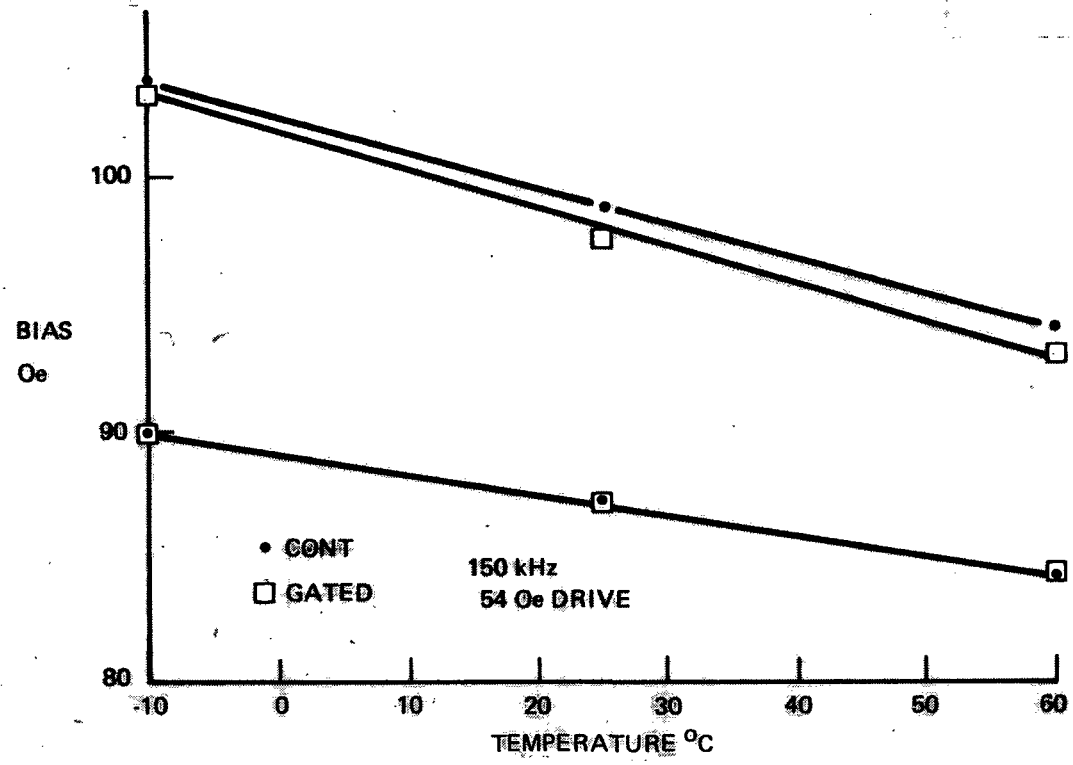


Figure 51. Comparison of Gated/First Bit Detection Operation (1 Cycle Percharge) and Continuous Operation (Over Temp)

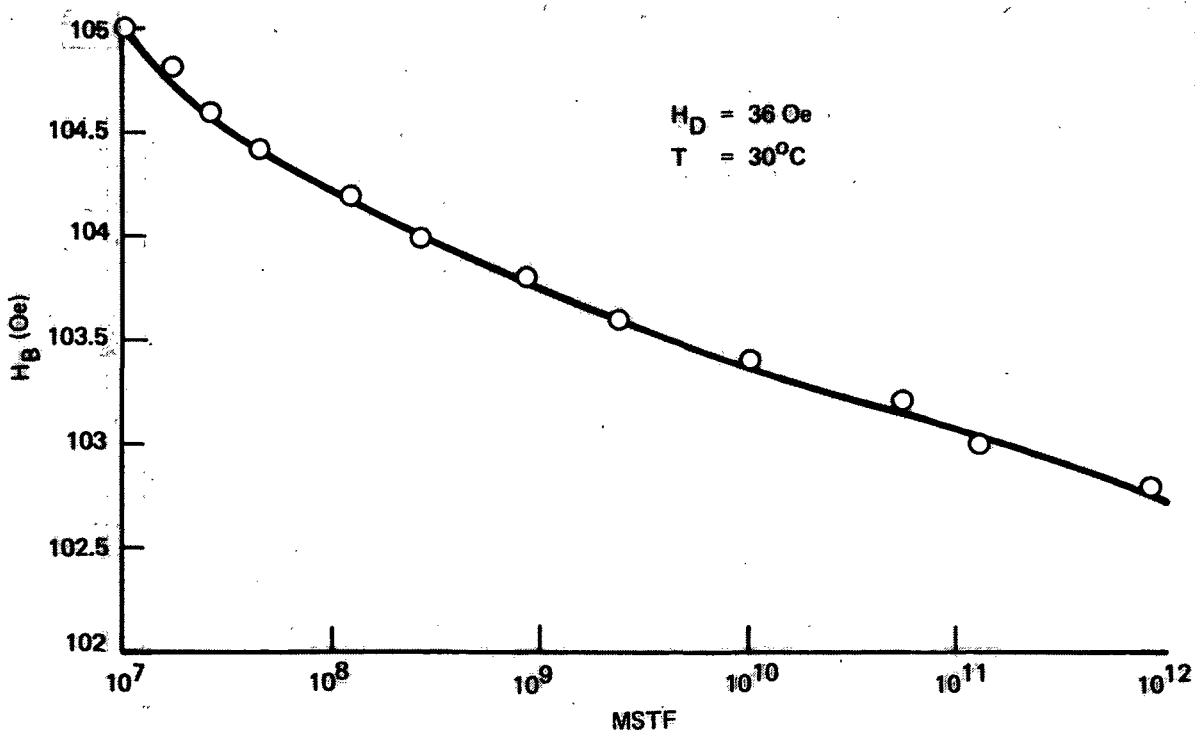


Figure 52. Variation of the Upper Margin for the M-1067B 100K Bit Chip as a Function of the Mean Step to Failure. (Lower Margin Edge $H_B \simeq$ 93 Oe at MTSF = 10^7 Steps.)

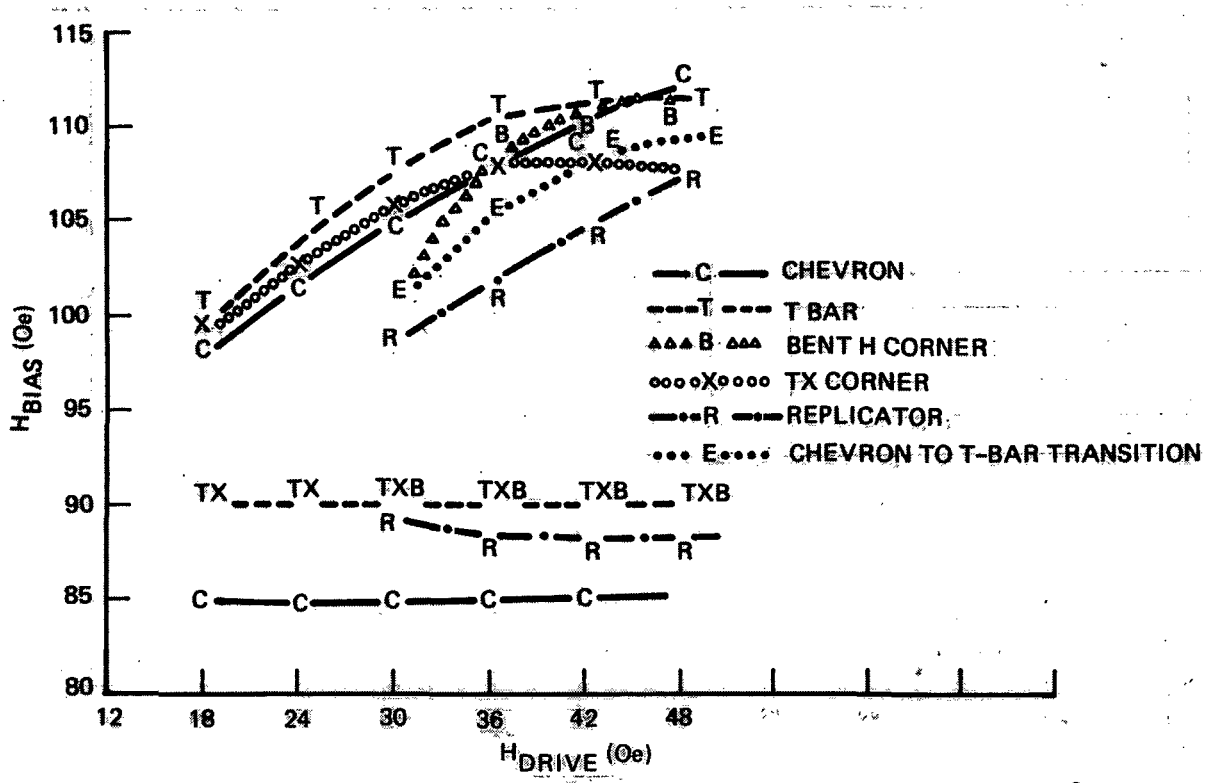


Figure 53. Component Margins for the M-1067B 100K Bit Chip (T = 25°C and 150 kHz Continuous)

Pulse amplitude variation over temperature for generation and annihilation in the 1067 design are shown in Figures 54a and 54b respectively. The multiple curves within each figure indicate the variation observed over a number of devices from different wafers and process runs. No maximum in pulse amplitude was observed for generation, however, currents higher than 250 to 300 ma were not possible with the test equipment employed in this measurement. The minimum limit on generation is for reliable generation; in general some sporadic bubble generation was observed down to 40 to 50 ma at 60°C. Above the maximum limit for annihilation, failure appears to be that of bubble shifting or sporadic generation at the outer edge of the annihilator loop. Below the minimum limit, failure to collapse the bubble is primarily the fault observed. In general, generation and annihilation are fairly insensitive to the pulse width. At 150 kHz the generator should be operated with at least 150 to 200 nsec width to reduce the amplitude required for operation. Pulse widths in the range of 200 nsec to 0.5 μsec will work satisfactorily for both operators over the temperature range - 10°C to 60°C.

Typical phase margins for all the operations of the 1067 design are shown in Figure 55. In general phase margins and phase position of all the operations are insensitive to temperature at 150 kHz. The shaded area is excluded from the operating region to avoid problems from the electrical transients associated with start/stop.

An expanded view of the 1067 detector and a typical output signal is shown in Figure 56. The room temperature sensitivity of this detector is .8 Mv/ma, and typical error rates obtained with this configuration are similar to those of Figure 49. The variation of the 100 element detector maximum and minimum sensitivity observed for a number of devices over the temperature range -10°C to +60°C is shown in Figure 57.

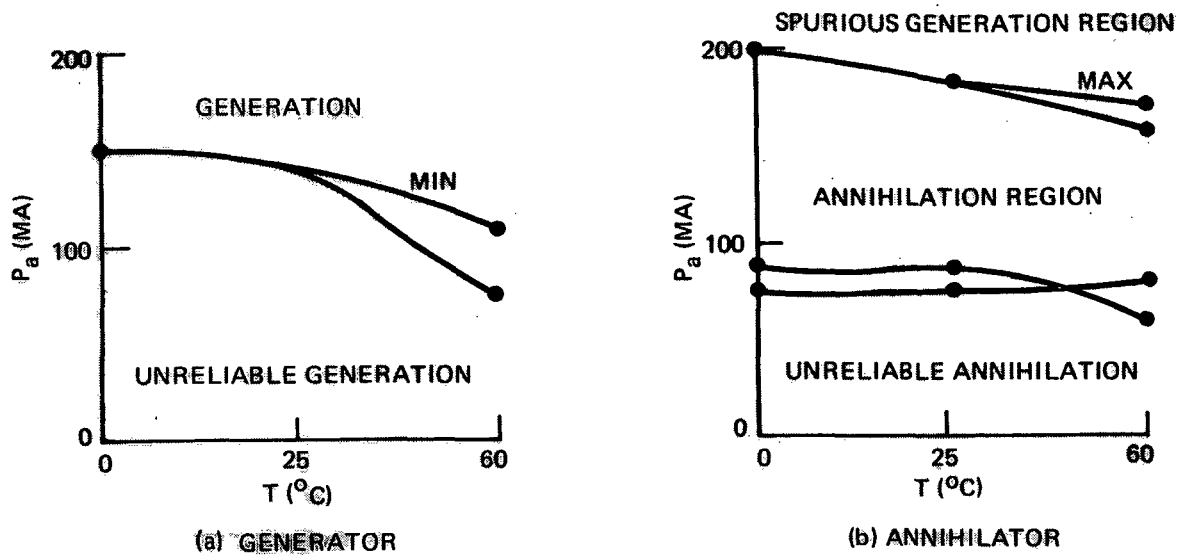


Figure 54. Generator and Annihilator Pulse Amplitude Variation with Temperature

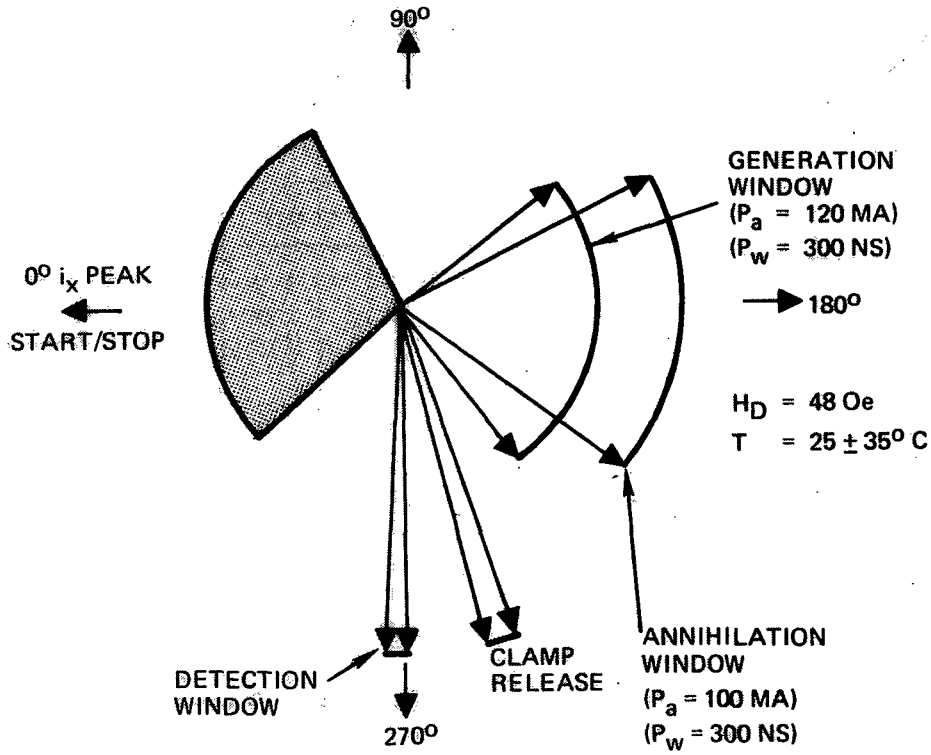


Figure 55. M-1067 Generator, Annihilator and Detector Phase Margins

Figure 56. Typical M-1067B 100K Bit Chip Chevron Detector Bubble and No Bubble Output (with no clamp)

The detailed structures of the one and zero signals over the temperature range and for various drive fields are shown in Figure 58 and 59. Although the detector sensitivity falls to 0.3 to 0.5 mv/ma at 60°C this value is still adequate to provide reliable, low error rate device operation.

A major concern related to multichip cell operation is the matching of detector windows of devices which are to share common sense electronics. The data in Figure 60 shows the overlap window of 6 devices from 4 different garnet wafers and 3 separate processes lots over a drive field range of 54 ± 9 Oe and two unclamp phasings. It can be seen that suitable detection windows (0.3 mv/ma min. sensitivities at 60°C) can be obtained for devices from different wafers (and process lots). Data on buildup of 8-chip carriers to be presented later will add further confirmation to the confidence level for multichip matching.

The phase diagram for the various M-1067 device functions is summarized in Figure 55. It can be seen that detection occurs 270 deg after the start/stop direction to provide as much time for domain stripout for first bit read as possible. The control functions of generation and annihilation have very wide phase margins, thus increasing the flexibility of the system designs. In summary, the conclusions of the design evaluation of the 1067 (1067B) chip are: (1) the basic design is sound and suitable for the prototype data recorder, (2) in gated operation reliable first bit read has been demonstrated from -10°C to -60°C with margins equivalent to continuous operation, (3) the passive replicator is the limiting component in the chip design, and (4) good temperature dependence of detectors and matching of detector characteristics has been achieved.

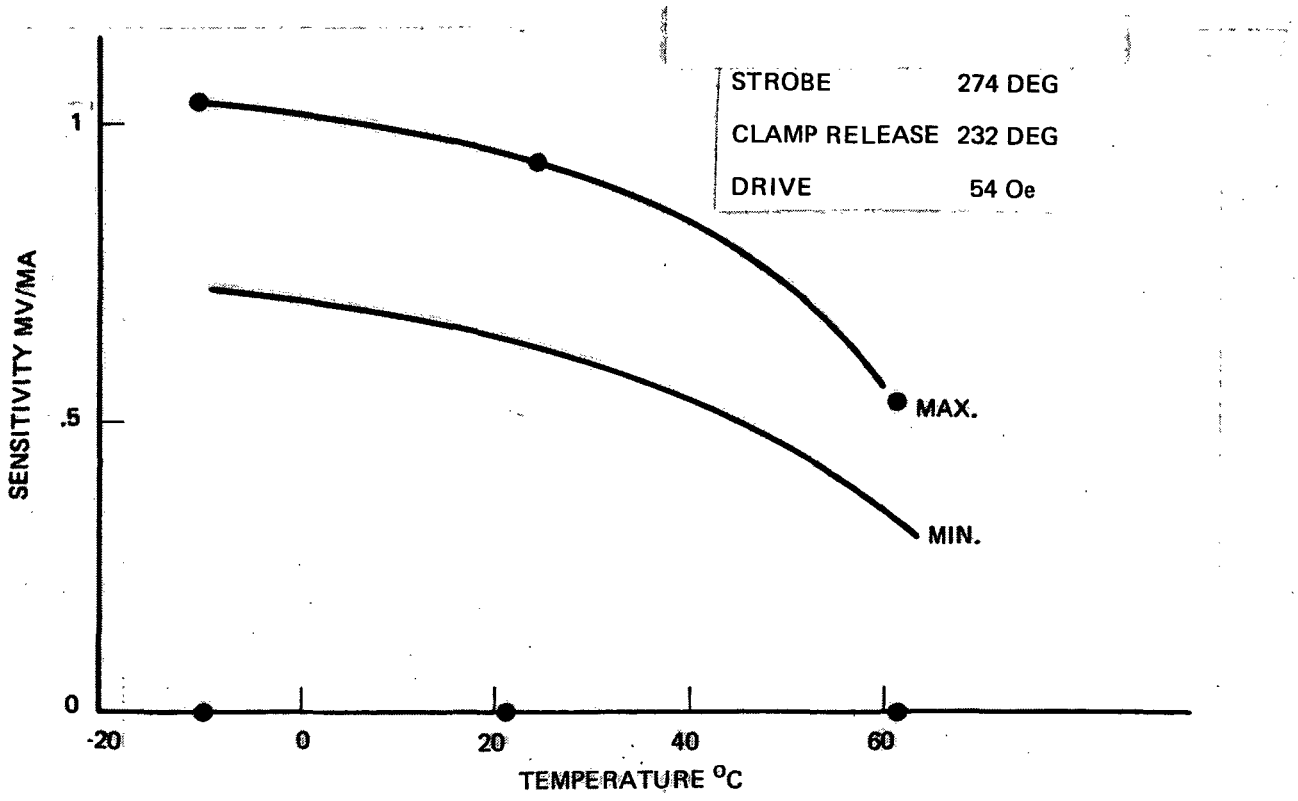


Figure 57. 1/O Detection Window Sensitivity Variation with Temperature (Minimum and maximum spread observed for a number of different chips)

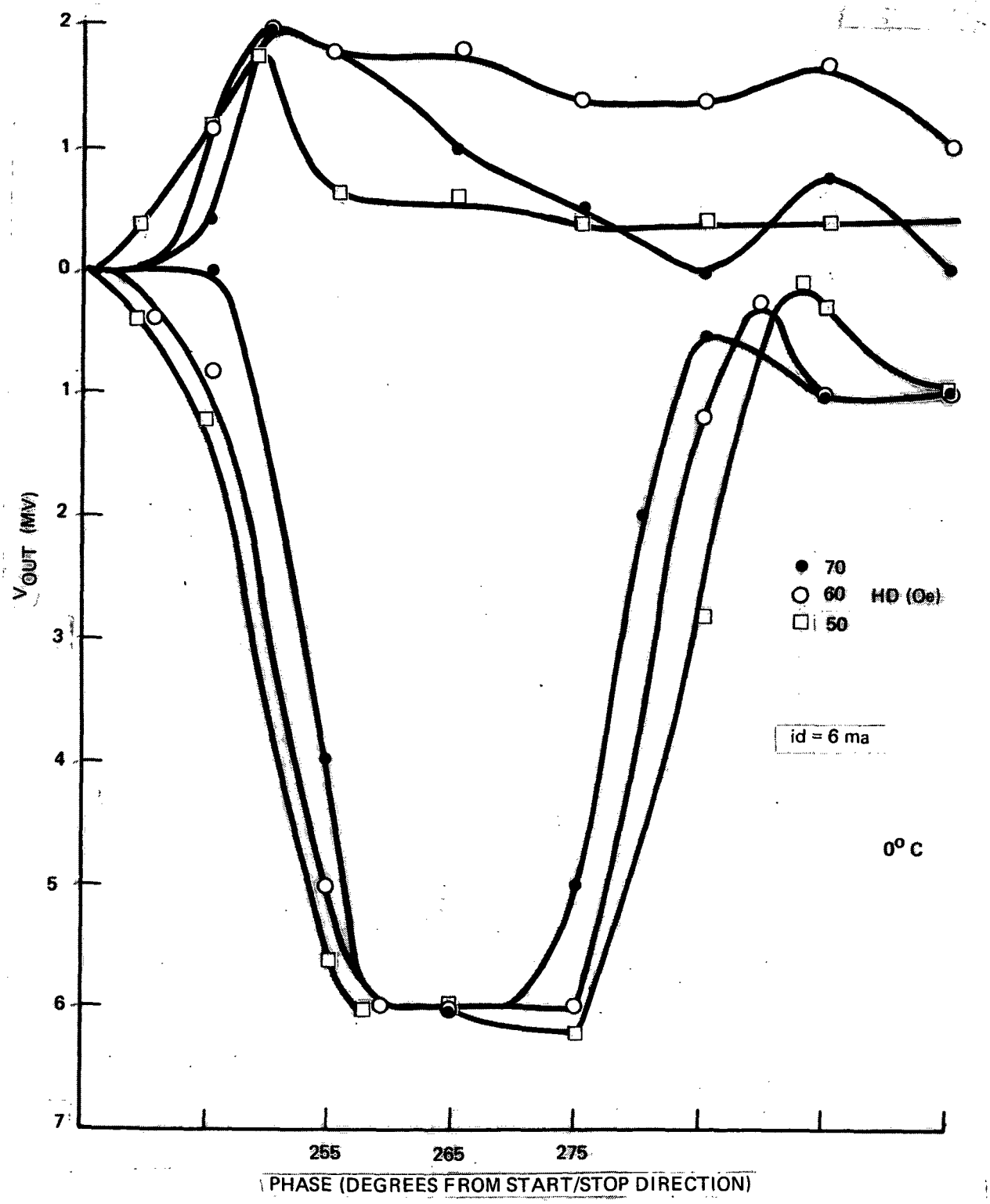


Figure 58. M-1067 Detector Signal Characteristic for Three In-Plane Drive Fields. Clamp Release at 235 deg. Upper curves are "0" signals and lower curves are "1" signal.

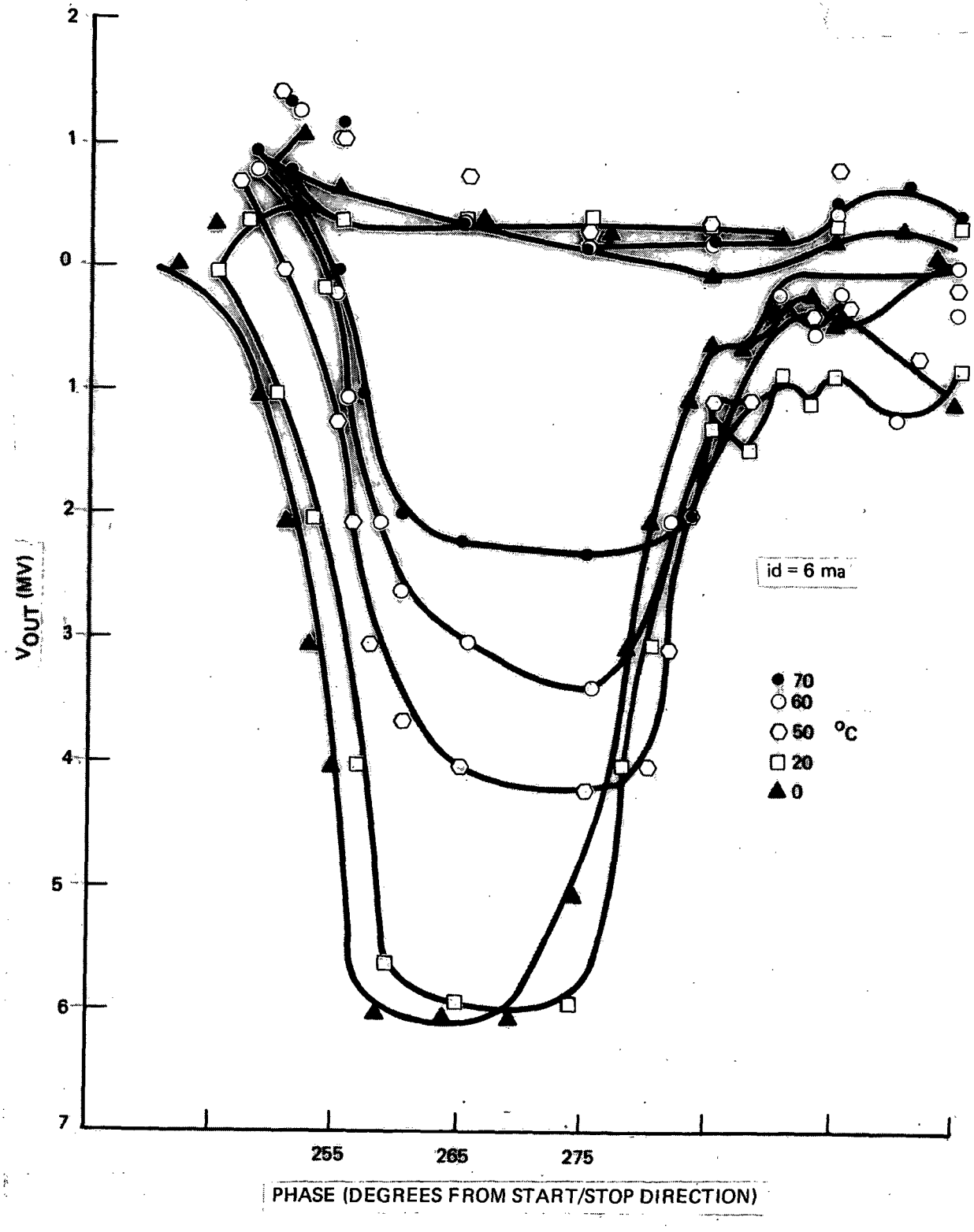


Figure 59. M-1067 Detector Signal Characteristic for Temperatures Between 0°C and 70°C. Clamp release at 235 deg.

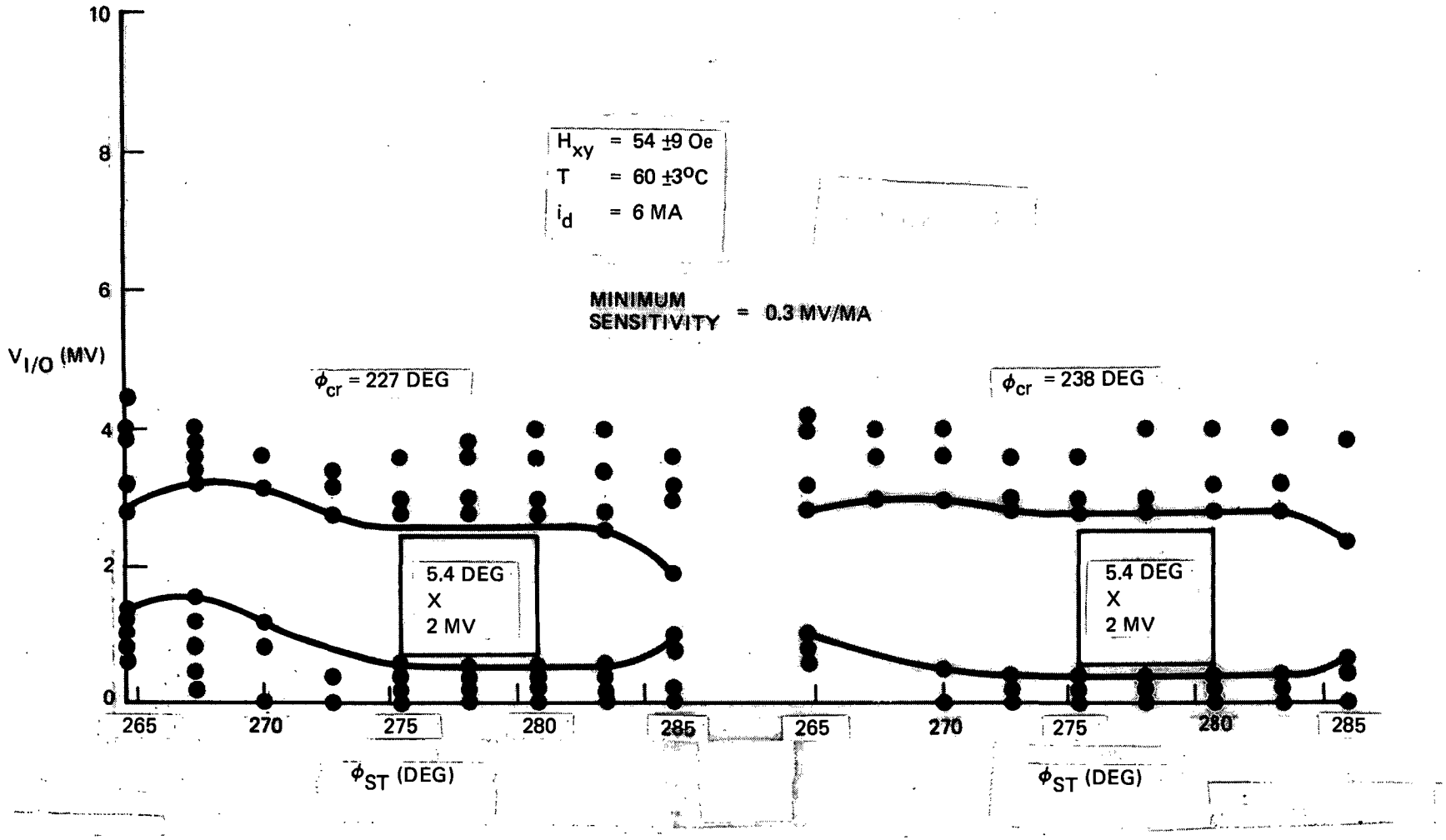


Figure 60. M-1067 Composite Detector Window Variation for Six Chips as Function of Strobe Phasing for Two Clamp Release Phasings. 0 ns is at 270 Degree Phase. (Box indicates Strobe/Clamp margin for a 0.3 mv/ma sensitivity at T = 60°C.)

7.3 Die Matching for Multichip Packages

Both systems presently employing the 100K bit serial chip, the Rockwell International POS/8 and the NASA 10^8 bit data recorder prototype, utilize (different) 8-chip carriers. In the data recorder system two of these carriers are used in a 16-chip cell design wherein all 16 chips are required to operate in common bias and rotating fields. The POS/8 system employs a single carrier in an 8 chip memory cell. In both systems the chips in a cell share common sense electronics. These multichip package designs for the system cells require close matching of the device properties so that suitable overlap of the operating ranges of the chips exists in order to provide reliable performance. This matching must also track uniformly over the temperature range of system operation.

The sequencing wafer prober described earlier is used to provide the device matching chip selection data for the multichip carrier. The results of wafer level tests of 100 kHz operation in the gated mode at 30°C and 60°C are examined for sets of chips which have maximum margin overlap acaoss the temperature range. After wafer scribe and break, eight of the chips identified for each set are mounted in a carrier and reprobed at 30°C and 60°C. If no handling damage has occurred wire bonds are made from the chip pads to the package metallization and the assembled carrier is passed on to cell test. If device degradation is detected at the carrier level test the damage dice are replaced.

This procedure has been used successfully to produce the matched devices to populate the first deliverable cells on the SSDR program and several POS/8 systems which have been delivered to government and commercial customers. Table 28 shows typical wafer and carrier level data at 30°C and 60°C for four 8-chip carriers. Results such as these provide confidence that suitable performance can be obtained in multi-chip packages, through a combination of well-matched film properties and well-controlled device processing. Note that carrier 114 contains dice from 5 different wafers. The first two numbers in the die no. column identify the wafer and the last one is the die number (example: $\underbrace{25\text{-}23C}_{\text{wafer}} - \underbrace{28}_{\text{die}}$).

7.4 Device Environmental Testing

Several types of environmental tests were performed on devices fabricated on this program. The primary objective of these tests was to identify possible failure modes, not to provide device acceptance criteria. Some environmental testing of chip/package configurations to evaluate die mounting/wire bonding techniques has already been described in Section 4. This section will cover the results of environmental tests on device functional properties. There were four basic types of environmental tests called for in the program viz:

1. Data retention during power shutdown
2. 2000 hr Life Test
3. Thermal Tests
4. Mechanical Tests

7.4.1 Data Retention. - The goal of the data retention test was to demonstrate the ability of the memory element to maintain a stored data pattern during a power shutdown duration of at least 24 hrs.

Three permanent magnet structures were used to operate three 100K bit (M-1050) devices at 0 deg, 25 deg and 50 deg C. First each device and coil set were brought to their specific operating temperature. Data was entered into all three devices and stable gated operation confirmed. The "off" gate was placed in manual and all power was removed for 24 hrs. During the 24 hrs the temperature of each structure was maintained to ±1°C of the specified ambient. After 24 hrs the devices were powered up in the gated mode and interrogated. It was confirmed that all three had retained the data that had been inserted prior to shutdown. This nonvolatility characteristic has since been confirmed many times with a demonstration unit of the POS/8 which has been carried through the U.S. and Western Europe without any data loss during power shutdown, system shipment and reactivation.

7.4.2 Life Test. - In an effort to demonstrate the long term performance of the memory element, a 2000 hr operating life test was conducted. This test was split into two segments, a propagation life portion and a generator-detector-annihilator life portion. In the propagation test the memory element content was periodically monitored for absence of propagation errors and detection malfunction. The memory elements were to be held at three separate temperatures throughout the 2000 hrs. To meet this requirement, six 20K bit versions of the M-1061 memory element were selected to be subjected to the 2000 propagation hour test. The devices were bonded to single chip boards and characterized at room temperature. Table 28 shows the pre-test margins.

The devices were placed in separate paired test structures with permanent magnet bias. Each test pair was stabilized at the specific operating temperature and 50 0e drive field. Device operation was then initialized and the permanent magnet bias was adjusted for near center margin for each device. A detector current of 4ma dc was continuously applied throughout the 2000 hr test. Throughout the test period, the data initially contained in the register was periodically changed to assure operation of the annihilator, and generator loops. The detected signal was similarly monitored. At ~575 hrs into the test, the exerciser pulse generating network failed and three device generators were burned out. The result left one complete device at each temperature. The remainder of the test proceeded without incident. At the conclusion of the life test the margins were remeasured. No differences beyond experimental error were noted.

Fifteen 100K bit (1050) memory elements were subjected to a 2000 hrs generators and the annihilator pulsing and detector excitation. The devices were separated into 3 groups of 5 each and placed in 3 separate thermally controlled chambers. The chambers were stabilized at 0 ± 2 deg, 25 ± 2 deg and 50 ± 2 deg C respectively. The control elements (annihilator, generator and detector) were exercised continuously for 2000 hrs. The annihilators were pulsed at 75 kHz with a 100-110 ma pulse 0.5 μsec wide. The generators were pulsed at 150 kHz with a pulse of 160 ma, 0.5 μsec wide. The detectors were subjected to an 8 to 10 ma dc excitation. Wave shapes, voltages and resistance monitored prior, during and subsequent to the test did not change. Optical microscopy of the loops and detectors revealed no indication of stress or electromigration.

TABLE 28. WAFER TO CARRIER MARGIN CORRELATION

Well No.	Die No.	T = 30°C Wafer ΔH (Oe)	T = 30°C Carrier	T = 60°C Wafer	T = 60°C Carrier
CARRIER: 114					
1	25-2G-17	97-109.5 = 12.5	98.5-109.9 = 11.4	94-104 = 10	92.1-102.1 = 10
2	25-23C-22	100-111 = 11	100-112.6 = 12.6	95-105 = 10	94.8-103.4 = 8.6
3	24-13F-18	96.3-111.6 = 15.3	97.4-108.8 = 11.4	92.6-105.3 = 12.7	92.7-101.4 = 8.7
4	24-10F-28	99.5-109.5 = 10	100-113.8 = 13.8	94-105 = 11	93.5-104.8 = 11.3
5	25-23C-20	97-112 = 15	97.3-112.6 = 15.3	94-108 = 14	93.5-102.2 = 8.7
6	25-23C-8	97-112 = 15	98.5-113.8 = 15.3	92.5-106.5 = 14	93.5-104.8 = 11.3
7	25-23C-28	100-113.5 = 13.5	100-112.6 = 12.6	94-105 = 11	93.5-103.4 = 10
8	25-9G-4	100-110.5 = 10.5	100-112.6 = 12.6	95-106.5 = 11	94.8-104.8 = 10
Overlap		100-109 = 9	100-108 = 8	95-104 = 9	95-101 = 6
CARRIER: 115					
1	24-23F-11	97.7-111.6 = 14	100.6-115.8 = 15.2	94-107.9 = 13.9	94.8-108.7 = 13.9
2	24-23F-25	97.7-113 = 15.3	99.3-117.3 = 18	94-107.9 = 13.9	94.8-107.5 = 12.7
3	25-7G-18	96.3-111.6 = 15.3	98.1-115.8 = 17.7	94-107.9 = 13.9	94.8-107.5 = 12.7
4	25-17K-28*	97.7-115.6 = 17.9	99.4-115.9 = 16.5	92.2-108.8 = 16.6	94.8-107.5 = 12.7
5	24-13F-26	96.3-110.4 = 14.1	98.1-110.6 = 12.5	92.6-104 = 11.4	93.4-102.1 = 8.7
6	24-13F-27	96.3-109 = 12.7	98.4-111.1 = 12.7	92.6-104 = 11.4	93.4-101 = 7.5
7	24-13F-28	96.3-111.6 = 15.3	98.4-111.1 = 12.7	92.6-105.3 = 12.7	93.5-103.5 = 10
8	24-13F-30	97.7-110.4 = 12.7	98.4-111.1 = 12.7	94-105.3 = 11.3	93.5-103.5 = 10
Overlap		98-109 = 9	101-110 = 9	94-104 = 10	95-101 = 6
CARRIER: 116					
1	25-48I-3	99-112.9 = 13.9	100-112.7 = 12.7	94.8-100.2 = 11.4	94.8-104.8 = 10
2	25-48I-5	96.3-111.6 = 15.3	97.4-111.3 = 13.9	94.8-106.2 = 11.4	93.4-104.8 = 11.4
3	25-48I-7	99-111.6 = 12.6	102.7-112.7 = 10	96.2-107.6 = 11.4	97.5-106.5 = 8.6
4	25-17K-16	989.-114.3 = 15.4	99.8-116.3 = 16.5	94.8-108.8 = 14	94-106.5 = 12
5	25-48I-29	99-112.9 = 13.9	98.6-113.9 = 15.3	93.5-106.2 = 12.7	94.8-106.1 = 11.3
6	25-17K-11	96.5-113.2 = 16.7	98.6-113.9 = 15.3	93.5-107.6 = 14.1	94.9-108.8 = 14
7	25-48I-19	99-111.6 = 12.6	100-112.7 = 12.7	94.8-106.1 = 11.4	94.8-106.1 = 11.3
8	25-48I-22	97.6-114.3 = 16.7	98.6-112.7 = 14.1	93.5-108.8 = 15.3	97.5-106.1 = 8.6
Overlap		99-111 = 12	103-111 = 8	97-106 = 9	98-104 = 6
CARRIER: 118					
1	25-48I-17	96.3-110.3 = 14	98.5-112.6 = 14.1	93.5-104.8 = 11.3	93.6-103.6 = 10
2	25-48I-28	101.6-114.3 = 12.7	101.2-113.9 = 12.7	94.8-108.8 = 14	96.3-106.3 = 10
3	25-15K-4	100.2-111.6 = 11.4	99.9-112.6 = 12.7	94.8-104.8 = 10	93.6-102.3 = 8.7
4	25-15K-5	99-112.6 = 13.9	99.9-113.9 = 14	94.8-104.8 = 10	93.6-103.6 = 10
5	25-15K-7	99-114.3 = 15.3	100-115.3 = 15.3	94.8-107.6 = 12.5	94.9-107.7 = 12.8
6	25-15K-13	100.2-114.3 = 14.1	101-115 = 14	96.2-108.8 = 12.6	95-107.6 = 11.6
7	25-15K-17	99-112.9 = 13.9	99.9-112.6 = 12.7	93.5-106.2 = 12.7	93.6-103.6 = 10
8	25-15K-16	100.2-111.6 = 11.4	100.8-111.9 = 11	96.2-106.2 = 10	95.5-102.5 = 7
Overlap		102-110 = 8	102-111 = 9	97-104 = 7	97-102 = 5

7.4.3 Thermal and Mechanical Tests. - Two of the M-1050 100K bit devices were mounted on polyimide-amide sheathed epoxy glass test boards (see Section 4) and subjected to the following sequence of mechanical and thermal environmental stresses:

1. Mechanical shock: 3000 g's for 0.5 msec.
2. Mechanical vibration. 30g, 20-20,000 cps along 3 axes with an amplification factor of unity.
3. Centrifuge: 2000g, 5000g and 10,000g on 3 axes.
4. Thermal cycle: 15 cycles - 5 min ≤ 0°C 5 min at +25°C, 5 min at 150°C. Transfer time less than 1 minute.
5. Thermal shock: 15 cycles - 5 min at 150°C and 5 min at 0°C with transfer time less than 5 seconds.

The device operating characteristics were measured at 150 kHz and room temperature before and after each test (including each g level of test 3). No change in device performance was observed at any stage of the testing.

8. COST PROJECTION FOR 100K BIT MEMORY ELEMENTS

One of the contract tasks was the performance of a cost projection for the bubble domain memory element based on the results shown in Chapter 6. This projection was performed and presented during an oral review at NASA (Ref 12). An updated summary of this projection will be presented in the following paragraphs.

A cost projection based on a fabrication run of 10,000 chips is contained in Table 29. It is assumed that the device fabrication is done in a production line such as that in our Special Devices Division which provides devices for Autonetics Group requirements. Three different values of yield are assumed to show the yield-dependent cost range. The data are based on a 16 μm period, 100K bit memory element. It can be seen that the garnet material is presently the largest single contribution to the die cost. The material cost consideration for large capacity memory elements are shown in Table 30. The cost advantages of going to larger diameter are evident from this table. Everything is referred to the 51 mm diameter wafers which are presently our standard size. The useful data is defined as that excluding a 2.5 mm annulus at the periphery of the wafer where the film thickness is nonuniform and defect density is high. Wafers of 76 mm diameter are just now becoming available and do not yet show the trend of lower cost/useful area for increasing diameter. However, the increase in number of die/wafer more than offsets the higher substrate price and the advantages should become more pronounced as 76 mm material reaches production quantities. The garnet film cost used in the Table 29 projection is $100, and an 80 percent mask yield is assumed. Thus the garnet material cost for 51 mm dia wafers for a 20 percent device yield is $\frac{\$100}{0.2 \times 34 \times 0.8} \approx \$18$. A photo comparing garnet films from 13 mm to 76 mm diameter is shown in Figure 61.

TABLE 29. COST PROJECTION FOR 100K BIT DEVICES

ITEM	COST/DIE ($) YIELD		
	20%	15%	10%
Yielded 51 mm dia. Garnet Wafers	18.00	27.00	36.00
Mask Sets	2.00	3.00	4.00
Device Processing*	12.00	15.00	24.00
Die Testing	3.00	3.00	3.00
Die Mounting & Bonding	2.00.	2.00	2.00
Total	37.00	47.00	69.00

*Includes Device Testing at Wafer Level

TABLE 30. MATERIAL COST CONSIDERATIONS FOR LARGE CAPACITY DEVICES

Substrate Diameter (mm)	25	38	51	76
Useful Wafer Area (%)	58	71	78	85
Cost for Useful Area*	2.3	1.3	1.0	1.97
10^5 Bit Devices/Wafer				
24 μm Period	2	5	12	27
16 μm Period	5	13	34	80
Material Cost/Die** (Unyielded)	14.7	3.2	1.0	0.84

*Polished Substrates, Normalized to 51 mm Dia
**16 μm Period, 16 Slices/cm, Normalized to 51 mm dia

The assumptions on mask costs are an average mask yield of 80 percent during a mask life of 20 contacts. The remaining figures are an extrapolation of our research lab costs to those of a production environment based on past experience. Based on the results of Chapter 6 a yield of 15 percent seems reasonable which would lead to a memory element cost of ~$50 or 50 millicents/bit for a serial 100K bit memory element using 16 μm period, 4 μm bubble technology in the 1977-1978 time frame.

Through incorporation of the improvements discussed in the next section it is estimated that the cost of bubble domain memory elements will be <10 millicents/bit by 1980.

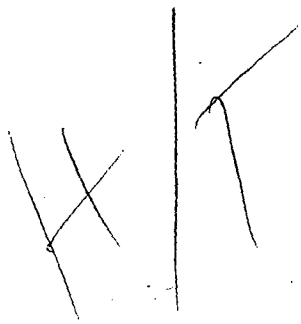


Figure 61. Bubble Domain Garnet Films on Wafers From 0.5 to 3.0 in. in Diameter

9. CONCLUSIONS AND RECOMMENDATIONS

The contents of the previous chapters have demonstrated that a memory element capable of meeting the performance and cost goals of NASA has been developed. Guidelines for the device design and the final realization of the memory element have been discussed in Chapter 2 and the performance characteristics have been presented in Chapter 7. The main improvement desired in the element performance would be a reduction in the operating drive field. Results of the fabrication runs described in Chapter 6 confirm that the 100K bit serial chip can be made with acceptable yields using the process described in Chapter 3.

In summary the major accomplishments of this program were:

1. Design, fabrication and operation of the first bubble domain memory element with a capacity of 100K bits (1974)

2. Development of a mask generation procedure for fabrication of durable high yield arrays of nonredundant patterns with 1 μm resolution over an area of 6.4 x 6.4 mm

3. Evolution of a process capable of fabricating serial 100K bit devices with high yield.

4. Demonstration of a producible high performance large capacity memory element through design and process modifications

5. Demonstration of the feasibility of matching chips from different process wafers and/or lots in multichip packages

Item 1 represented almost an order of magnitude increase in capacity over previously reported bubble domain devices. The first 100K bit chips had rather poor performance (by today's standards) and the yield, though encouraging for a first effort, was limited by certain obvious shortcomings in the mask generation and device processing procedures/facilities. The modifications in pattern generation, mask generation, mask fabrication and device processing represented by Items 2 and 3 have been presented in the body of this report. These accomplishments upgraded the pattern yield and allowed the introduction of some design changes which were not feasible previously. Further design changes and processing experience resulted in a final chip (M-1067B) with excellent performance and producibility, i.e., the accomplishment of Item 4. The third yield run and subsequent fabrication runs have established the capability of the device/process to provide chips with matched performance over a wide temperature range in a multichip package.

In spite of the success achieved on this program, evaluation of the overall effort indicates some areas where further advances could lead to much improved yield (lower cost) as well as better device performance.

The most troublesome aspects of the present technology are:

1. Achieving perfect 10X reticules for the mask generation
2. Obtaining high mask pattern yield with 1 μm resolution
3. Processing large area non-redundant devices with 1 μm resolution
4. Reducing the device operating drive field

It is recommended that future large capacity device developments be directed along the following lines to improve performance and reduce cost.

1. Develop three inch diameter garnet wafers as the standard material size.
2. Replace existing T-bar propagation circuits with improved structures such as the gap tolerant half disk elements (Ref 27, 28) or asymmetric chevrons (Ref. 29).
3. Design memory elements incorporating a small degree (~10 percent) of redundancy

The motivation and impact of (1) is obvious from Table 30. The improved propagation structures offer two options in device development - increased capacity with the same resolution or reduced resolution with the same capacity. The latter option may also open the possibility of going to projection printing which was not feasible for a 100K bit chip needing 1 μm resolution. The half disk structures have also shown, in small capacity circuits, lower drive fields than the T-bar structures. Finally, the data of Chapter 6 shows that although respectable yields can be obtained with a non-redundant design, dramatic improvements in yield can be expected by incorporating a small degree of redundancy in the chip design. This will have the additional benefits of relaxing the need for a perfect 10X reticule and increase the mask fabrication yield. Of course, as has been pointed out previously, one must evaluate the consequences of a redundant design in terms of the overall system application and determine that the tradeoff of increased processing yield for increased complexity in testing and system electronics is favorable for the case in question.

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